# Product Specification

800G DR4 OSFP224 Flat Top PAM4 1310nm 500m DOM MTP/MPO-12 APC Optical Transceiver Module

PN: OSFP-800G-DR4



## Features

- Hot-pluggable OSFP224 Flat Top form factor
- Aggregate data rate of 850Gb/s
- 4 × 212.5Gb/s PAM4 host electrical lanes
- 4 × 212.5Gb/s PAM4 optical lanes
- Single +3.3V power supply
- MTP/MPO-12 APC connector
- Maximum power consumption ≤15.0W
- Four parallel 1310nm optical lanes
- Up to 500m over G.652 single-mode fiber
- 4-channel PIN/TIA receiver array
- Built-in digital diagnostic monitoring
- Host-side FEC supported
- Commercial case temperature range of 0°C to 70°C

## Compliance

- OSFP MSA
- Designed in alignment with IEEE P802.3dj
- Draft requirements for 800GBASE-DR4 and 800GAUI-4
- CMIS Rev. 5.0
- RoHS
- Class 1 Laser Product

## Applications

- 800G ConnectX-8 adapter interconnects
- 800G Ethernet and RoCE links
- AI and HPC cluster interconnects
- High-density server-to-switch links

## Description

The OSFP-800G-DR4 is a hot-pluggable OSFP224 Flat Top optical transceiver designed for high-speed 800Gb/s links over parallel single-mode fiber. The module uses four PAM4 host electrical lanes operating at 106.25 GBd per lane, corresponding to approximately 212.5 Gb/s per lane and an aggregate data rate of 850 Gb/s. The optical interface also uses four parallel 200G-class PAM4 lanes operating around 1310nm and supports transmission distances of up to 500 meters over G.652 single-mode fiber through a single MTP/MPO-12 APC connector.

The module uses parallel optics rather than wavelength multiplexing. Eight active fibers within the MTP/MPO-12 interface provide four transmit and four receive optical channels. The receiver incorporates a four-channel PIN photodiode and TIA array. The host-side interface uses four 200G-class PAM4 electrical lanes suitable for OSFP224 224G/lane host architectures.

The module operates from a single 3.3V power supply with a maximum power consumption of 15.0W and supports a commercial case temperature range of 0°C to 70°C. Digital diagnostic monitoring and module control are provided through the two-wire management interface. Host-side FEC is used to achieve the required link performance.

## Product performance Specifications

### 1、Absolute Maximum Ratings

| Parameter | Symbol | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|
| Storage Temperature | TS | -40 | | +85 | °C |
| Supply Voltage | VCC | -0.5 | | 3.6 | V |
| Relative Humidity, Non-condensing | RH | 5 | | 85 | % |
| Control Input Voltage | VI | -0.3 | | VCC + 0.5 | V |

### 2、Recommended Operating Conditions

| Parameter | Symbol | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|
| Operating Case Temperature | TC | 0 | | 70 | °C |
| Power Supply Voltage | VCC | 3.135 | 3.3 | 3.465 | V |
| Maximum Power Dissipation | PD | | | 15.0 | W |
| Aggregate Data Rate | DR | | 850 | | Gb/s |
| Electrical Lanes | | | 4 | | lanes |
| Electrical Bit Rate per Lane | | | 212.5 | | Gb/s |
| Electrical Signaling Rate per Lane | | | 106.25 ±50ppm | | GBd |
| Optical Lanes | | | 4 | | lanes |

| | | | | | |
|---|---|---|---|---|---|
| Optical Bit Rate per Lane | | | 212.5 | | Gb/s |
| Optical Signaling Rate per Lane | | | 106.25 ±50ppm | | GBd |
| Modulation Format | | | PAM4 | | |
| Two-Wire Serial Interface Clock Rate | | 100 | | 1000 | kHz |
| Power Supply Noise Tolerance | | | | 25 | mV |
| Rx Differential Data Output Load | | | 100 | | Ω |
| Operating Distance over G.652 SMF | | 2 | | 500 | m |

## 3、Host Electrical Interface

| Parameter | Value |
|---|---|
| Number of Electrical Lanes | 4 |
| Bit Rate per Lane | 212.5Gb/s |
| Signaling Rate per Lane | 106.25GBd ±50ppm |
| Modulation Format | PAM4 |
| Host Interface Architecture | 4×200G-class PAM4 |
| Form Factor | OSFP224 |

## 4、Transmitter Optical Characteristics — Per Lane

| Parameter | Symbol | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|
| Signaling Rate | | | 106.25 ±50ppm | | GBd |
| Modulation Format | | | PAM4 | | |
| Lane Wavelength Range | λC | 1304.5 | 1311 | 1317.5 | nm |
| Side-Mode Suppression Ratio | SMSR | 30 | | | dB |
| Total Average Launch Power | | | | 10 | dBm |
| Average Launch Power, Each Lane | TxAVG | -3.1 | | +4.0 | dBm |
| OMAouter, Each Lane | OMAmax | | | +4.2 | dBm |
| OMAouter, max(TECQ,TDECQ) <0.9dB | OMAmin | -0.1 | | | dBm |
| OMAouter, 0.9≤max(TECQ,TDECQ)≤3.4dB | OMAmin | -1.0 + max(TECQ,TDECQ) | | | dBm |

| | | | | | |
|---|---|---|---|---|---|
| TDECQ | TDECQ | | | 3.4 | dB |
| TECQ | TECQ | | | 3.4 | dB |
| \|TDECQ-TECQ\| | | | | 2.5 | dB |
| Transmitter Overshoot and Undershoot | | | | 22 | % |
| Transmitter Power Excursion | | | | 2.3 | dB |
| Average Launch Power of OFF Transmitter | | | | -15 | dBm |
| Extinction Ratio | ER | 3.5 | | | dB |
| Transmitter Transition Time | | | | 8 | ps |
| RIN21.4OMA | RIN | | | -139 | dB/Hz |
| Optical Return Loss Tolerance | ORL | | | 21.4 | dB |
| Transmitter Reflectance | TR | | | -26 | dB |

## 5、Receiver Optical Characteristics — Per Lane

| Parameter | Symbol | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|
| Signaling Rate | | | 106.25 ±50ppm | | GBd |
| Modulation Format | | | PAM4 | | |
| Lane Wavelength Range | λR | 1304.5 | 1311 | 1317.5 | nm |
| Damage Threshold | AOPD | +5.0 | | | dBm |
| Average Receive Power | RxAVG | -6.4 | | +4.0 | dBm |
| Receive Power (OMAouter) | RxOMA | | | +4.2 | dBm |
| Receiver Reflectance | RR | | | -26 | dB |
| Receiver Sensitivity, TECQ <0.9dB | SEN | | | -3.4 | dBm |
| Receiver Sensitivity, 0.9≤TECQ≤SECQ | SEN | | | -4.3 + TECQ | dBm |
| Stressed Receiver Sensitivity | SRS | | | -0.9 | dBm |

## 6、Stressed Receiver Test Conditions

| Parameter | Value | Unit |
|---|---|---|
| Stressed Eye Closure for PAM4 (SECQ) | 3.4 | dB |
| OMAouter of Each Aggressor Lane | 2.9 | dBm |

**Note 1:** Average launch power, each lane (minimum), is informative and is not the principal indicator of transmitter signal strength.

**Note 2:** Transmitter reflectance is defined looking into the transmitter.

**Note 3:** Receiver sensitivity (OMAouter), each lane, is informative and is defined as -3.4 dBm for TECQ below 0.9 dB and -4.3 + TECQ dBm for TECQ from 0.9 dB up to SECQ.

**Note 4:** Stressed receiver sensitivity is measured using a conformant PAM4 test signal at TP3 with the applicable pre-FEC error-rate criterion.

**Note 5:** The MTP/MPO-12 APC optical interface uses eight active fibers, consisting of four transmit fibers and four receive fibers.

**Note 6:** The module uses four parallel 200G-class optical lanes around 1310nm and does not use CWDM wavelength multiplexing.

## Recommended Host Board Power Supply Circuit

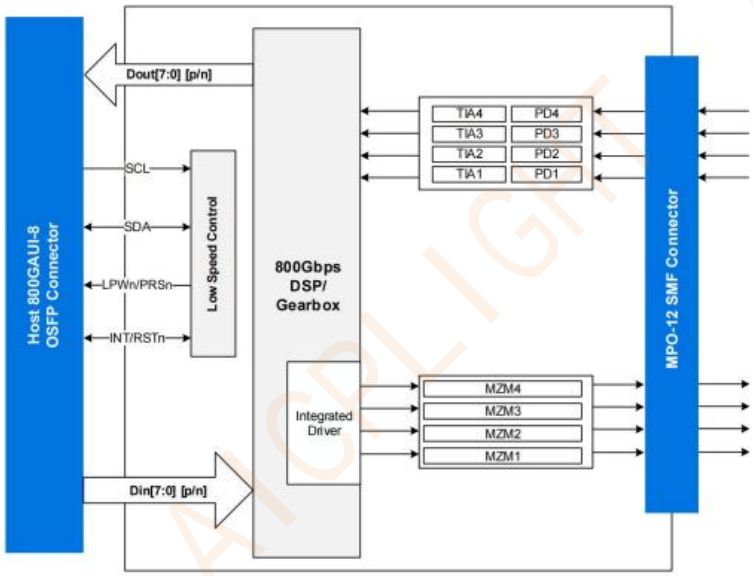


**Figure 1:**Module Block Diagram

## Optical Interface

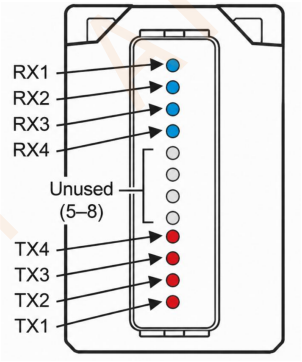


Figure3:Optical Lane Sequence

## Pin-out Definition




Figure4:Pin view(OSFP)

## Pin Function Definitions

| Pin | Logic | Symbol | Description | Note |
|---|---|---|---|---|
| 1 | | GND | Ground | |
| 2 | CML-I | TX2p | Transmitter Data Non-Inverted | |
| 3 | CML-I | TX2n | Transmitter Data Inverted | |

| | | | | |
|---|---|---|---|---|
| 4 | | GND | Ground | |
| 5 | CML-I | TX4p | Transmitter Data Non-Inverted | |
| 6 | CML-I | TX4n | Transmitter Data Inverted | |
| 7 | | GND | Ground | |
| 8 | CML-I | TX6p | Transmitter Data Non-Inverted | |
| 9 | CML-I | TX6n | Transmitter Data Inverted | |
| 10 | | GND | Ground | |
| 11 | CML-I | TX8p | Transmitter Data Non-Inverted | |
| 12 | CML-I | TX8n | Transmitter Data Inverted | |
| 13 | | GND | Ground | |
| 14 | LVCMOS-I/O | SCL | 2-wire Serial interface clock | 1 |
| 15 | | VCC | +3.3V Power | |
| 16 | | VCC | +3.3V Power | |
| 17 | Multi-Level | LPWn/PRSn | Low-Power Mode / Module Present | 2 |
| 18 | | GND | Ground | |
| 19 | CML-O | RX7n | Receiver Data Inverted | |
| 20 | CML-O | RX7p | Receiver Data Non-Inverted | |
| 21 | | GND | Ground | |
| 22 | CML-O | RX5n | Receiver Data Inverted | |
| 23 | CML-O | RX5p | Receiver Data Non-Inverted | |
| 24 | | GND | Ground | |
| 25 | CML-O | RX3n | Receiver Data Inverted | |
| 26 | CML-O | RX3p | Receiver Data Non-Inverted | |
| 27 | | GND | Ground | |
| 28 | CML-O | RX1n | Receiver Data Inverted | |
| 29 | CML-O | RX1p | Receiver Data Non-Inverted | |
| 30 | | GND | Ground | |
| 31 | | GND | Ground | |
| 32 | CML-O | RX2p | Receiver Data Non-Inverted | |
| 33 | CML-O | RX2n | Receiver Data Inverted | |
| 34 | | GND | Ground | |
| 35 | CML-O | RX4p | Receiver Data Non-Inverted | |
| 36 | CML-O | RX4n | Receiver Data Inverted | |
| 37 | | GND | Ground | |
| 38 | CML-O | RX6p | Receiver Data Non-Inverted | |
| 39 | CML-O | RX6n | Receiver Data Inverted | |
| 40 | | GND | Ground | |
| 41 | CML-O | RX8p | Receiver Data Non-Inverted | |
| 42 | CML-O | RX8n | Receiver Data Inverted | |
| 43 | | GND | Ground | |

| | | | | |
|---|---|---|---|---|
| 44 | Multi-Level | INT/RSTn | Module Interrupt / Module Reset | 2 |
| 45 | | VCC | +3.3V Power | |
| 46 | | VCC | +3.3V Power | |
| 47 | LVCMOS-I/O | SDA | 2-wire Serial interface data | 1 |
| 48 | | GND | Ground | |
| 49 | CML-I | TX7n | Transmitter Data Inverted | |
| 50 | CML-I | TX7p | Transmitter Data Non-Inverted | |
| 51 | | GND | Ground | |
| 52 | CML-I | TX5n | Transmitter Data Inverted | |
| 53 | CML-I | TX5p | Transmitter Data Non-Inverted | |
| 54 | | GND | Ground | |
| 55 | CML-I | TX3n | Transmitter Data Inverted | |
| 56 | CML-I | TX3p | Transmitter Data Non-Inverted | |
| 57 | | GND | Ground | |
| 58 | CML-I | TX1n | Transmitter Data Inverted | |
| 59 | CML-I | TX1p | Transmitter Data Non-Inverted | |
| 60 | | GND | Ground | |

**Note1:**Open-Drain with pull up resistor on Host.

**Note2:**See pin description for required circuit.

## Monitoring Specification

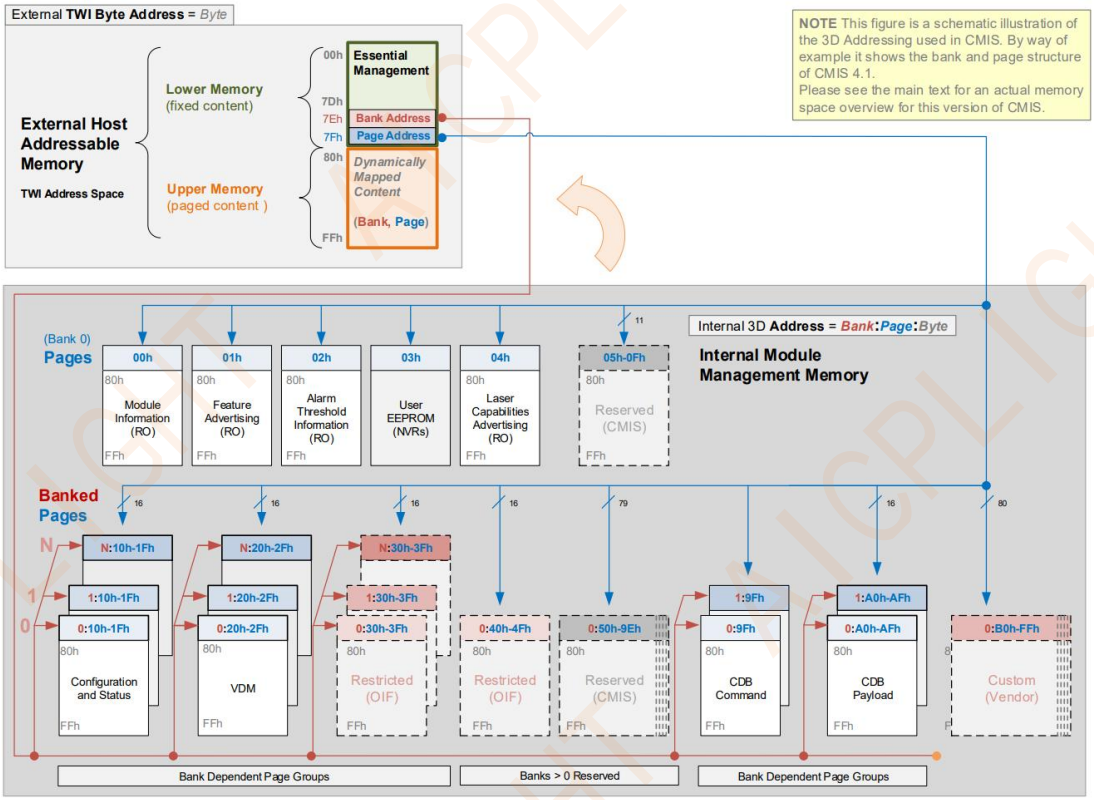


**Figure5:**Memory map

## Memory map Table

| Byte | Unit | Name | Description |
|---|---|---|---|
| | | **Lower Page 00h** | |
| 0-2 | 3 | Management Characteristics | Basic Information about how this module is managed |
| 3 | 1 | Global Status Information | Current state of Module, Interrupt signal status |
| 4-7 | 4 | Flag Summary | Summary of Flags set on specific Pages (and Banks) |
| 8-13 | 6 | Module-Level Flags | Flags that are not lane or Data Path specific |
| 14-25 | 12 | Module-Level Monitors | Monitors that are not lane or Data Path specific |
| 26-30 | 5 | Module-Level Controls | Controls applicable to the module as a whole |
| 31-36 | 6 | Module-Level Masks | Mask bits for the Module-Level Flags |
| 37-38 | 2 | CDB Command Status | Status of current CDB command |
| 39-40 | 2 | Module Active Firmware Version | Module Active Firmware Version number |
| 41 | 1 | Fault Information | Fault cause for entering ModuleFault state |
| 42-63 | 22 | | Reserved |
| 64-84 | 21 | | Custom |
| 85-117 | 33 | Supported Applications Advertising | Applications supported by module Data Path(s) |
| 118-125 | 8 | Password Facilities | Password Entry and Change (mechanism only) |
| 126-127 | 2 | Page Mapping | Page mapping into host addressable Upper Memory |
| | | **Upper Page 00h** | |
| 128 | 1 | SFF8024IdentifierCopy | Copy of Byte 00h:0 |
| 129-144 | 16 | VendorName | Vendor name (ASCII) |
| 145-147 | 3 | Vendor OUI | Vendor IEEE company ID |
| 148-163 | 16 | Vendor PN | Part number provided by vendor (ASCII) |
| 164-165 | 2 | Vendor Rev | Revision level for part number provided by vendor (ASCII) |
| 166-181 | 16 | Vendor SN | Vendor Serial Number (ASCII) |
| 182-189 | 8 | DateCode | Manufacturing Date Code (ASCII) |
| 190-199 | 10 | CLEICode | Common Language Equipment Identification Code (ASCII) |
| 200-201 | 2 | ModulePowerCharacteristics | Module power characteristics |
| 202 | 1 | CableAssemblyLinkLength | Cable length (for cable assembly modules only) |
| 203 | 1 | ConnectorType | Connector type of the media interface |
| 204-209 | 6 | Copper Cable Attenuation | Attenuation characteristics (passive copper cables only) |
| 210 | 1 | MediaLaneInformation | Supported near end media lanes (all modules) |
| 211 | 1 | Cable Assembly Information | Far end modules information (cable assemblies only) |
| 212 | 1 | MediaInterfaceTechnology | Information on media side device or cable technology |
| 213-220 | 8 | | Reserved |
| 221 | 1 | | Custom |
| 222 | 1 | PageChecksum | Page Checksum over bytes 128-221 |
| 223-255 | 33 | | Custom |

## Mechanical Dimension

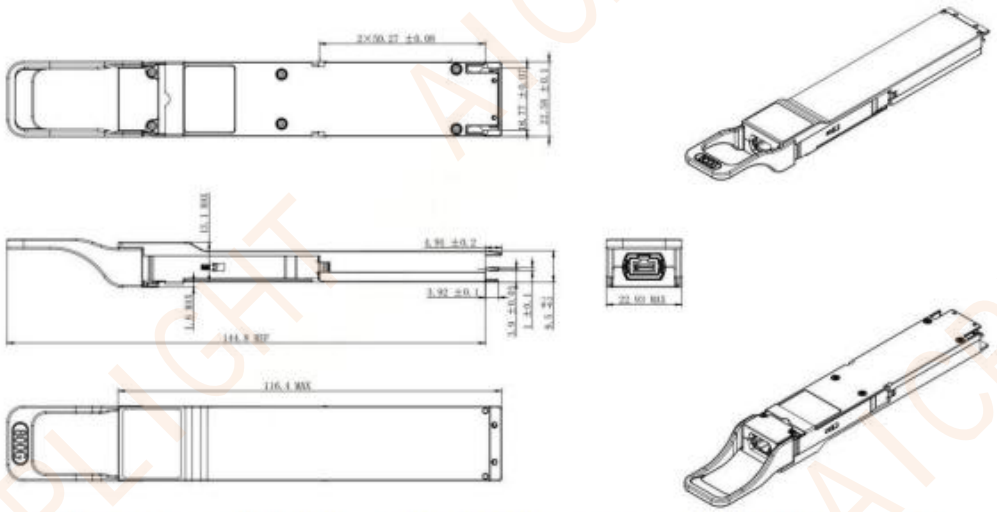

Figure 8 Mechanical Package Outline (All dimensions in mm) (Riding Heat Sink)




## Handling and Safety Precautions：

- **ESD Protection:** Use proper electrostatic discharge (ESD) protection when handling, installing, or removing the module.
- **Installation and Removal:** Insert or remove the OSFP module using the pull tab or release mechanism. Do not force the module into the cage or pull on the fiber cable.
- **Form Factor Compatibility:** OSFP Flat Top and OSFP Finned Top modules are designed for different thermal and cage configurations and are not interchangeable. Always use the module type specified for the host system.
- **Thermal Management:** Ensure sufficient airflow and proper heatsink contact. Do not obstruct the module or system cooling path, as the module may become hot during operation.
- **Connector Cleaning:** Keep MTP/MPO or LC optical interfaces clean and protected with dust caps when not in use. Clean connector end faces before connection.
- **Fiber Handling:** Avoid excessive bending, pulling, twisting, or crushing of fiber cables. Follow the specified minimum bend radius.
- **Laser Safety:** Do not look directly into the optical port or connected fiber while the module is powered. Do not disassemble or modify the module.

## Ordering Information

| PN | Description |
|---|---|
| OSFP-1.6T-2DR4 | 1.6T 2×DR4/DR8 OSFP224 Finned Top PAM4 1310nm 500m DOM Dual MTP/MPO-12 APC SMF Optical Transceiver Module |
| OSFP-1.6T-2FR4 | 1.6T 2×FR4/FR8 OSFP224 Finned Top PAM4 1310nm 2km DOM Dual Dual Duplex LC/UPC SMF Optical Transceiver Module |
| OSFP-800G-DR4 | 800G DR4 OSFP224 Flat Top PAM4 1310nm 500m DOM MTP/MPO-12 APC Optical Transceiver Module |