Product Specification

400GBASE-SR4 QSFP112 PAM4 850nm 50m DOM MTP/MPO-12 APC MMF Optical Transceiver Module

PN: Q112-400G-SR4



Features

- Hot-pluggable QSFP112 form factor
- Aggregate data rate of 425Gb/s
- 4 × 106.25Gb/s PAM4 host electrical lanes
- 4 × 106.25Gb/s PAM4 optical lanes
- Single +3.3V power supply
- MTP/MPO-12 APC connector
- Maximum power consumption ≤9.0W
- Up to 30m over OM3 MMF
- Up to 50m over OM4 MMF
- 4-channel 850nm VCSEL array
- 4-channel PIN receiver array
- Built-in digital diagnostic monitoring
- Requires host-side RS(544,514) FEC
- Commercial case temperature range of 0°C to 70°C

Compliance

- QSFP112 MSA
- IEEE 802.3db (400GBASE-VR4)
- IEEE 802.3ck (400GAUI-4 C2M)
- CMIS 5.0
- RoHS
- Class 1 Laser Product

Applications

- 400G Ethernet links
- QSFP112 NIC and DPU connections
- Data center interconnects
- AI and HPC cluster interconnects
- High-density server-to-switch links

Description

The Q112-400G-SR4 is a hot-pluggable QSFP112 optical transceiver designed for short-reach 400Gb/s links over parallel multimode fiber. It uses four independent PAM4 electrical lanes operating at 53.125 GBd per lane, corresponding to 106.25 Gb/s per lane and an aggregate data rate of 425 Gb/s. The module supports transmission distances of up to 30 meters over OM3 MMF and 50 meters over OM4 MMF through an MTP/MPO-12 APC optical interface.

The optical transmitter uses a four-channel 850nm VCSEL array, while the receiver incorporates a four-channel PIN photodiode array. Eight active fibers within the MTP/MPO-12 interface provide four transmit and four receive optical lanes. The host-side electrical interface uses four 100G-class PAM4 lanes compatible with the 400GAUI-4 architecture.

The module operates from a single 3.3V power supply with a maximum power consumption of 9.0W and supports a commercial case temperature range of 0°C to 70°C. Digital diagnostic monitoring and module control are provided through the 2-wire management interface. Host-side RS(544,514) FEC is required for operation.

Product performance Specifications

1、Absolute Maximum Ratings

Parameter	Symbol	Min	Typ.	Max	Unit
Storage Temperature	TS	-40		85	°C
Supply Voltage	VCC	-0.5		3.6	V
Relative Humidity, Non-condensing	RH	5		95	%
Control Input Voltage	VI	-0.3		VCC + 0.5	V

2、Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit
Operating Case Temperature	TC	0		70	°C
Power Supply Voltage	VCC	3.135	3.3	3.465	V
Maximum Power Consumption	PD			9.0	W
Aggregate Data Rate	DR		425		Gb/s
Electrical Lanes			4		lanes
Bit Rate per Lane			106.25		Gb/s
Signaling Rate per Lane	SRL		53.125 ±100ppm		GBd
Modulation Format			PAM4		
Operating Distance on OM3 MMF		0.5		30	m

Operating Distance on OM4 MMF		0.5		50	m
Pre-FEC Bit Error Ratio	BER			2.4×10^{-4}	
FEC			Host-side RS(544,514)		
Two-Wire Serial Interface Clock Rate				400	kHz
Rx Differential Data Output Load			100		Ω

3、Low-Speed Management Interface

Parameter	Symbol	Min	Typ.	Max	Unit
Module Output SCL/SDA Low Voltage	VOL	0		0.4	V
Module Output SCL/SDA High Voltage	VOH	VCC - 0.5		VCC + 0.3	V
Module Input SCL/SDA Low Voltage	VIL	-0.3		VCC × 0.3	V
Module Input SCL/SDA High Voltage	VIH	VCC × 0.7		VCC + 0.5	V

4、High-Speed Electrical Characteristics

Parameter	Min	Typ.	Max	Unit
Signaling Rate per Lane		53.125 ±100ppm		GBd
Modulation Format		PAM4		
Differential Peak-to-Peak Input Voltage Tolerance	750			mV
Differential Termination Mismatch			10	%
Single-Ended Voltage Tolerance Range	-0.4		3.3	V
DC Common-Mode Input Voltage	-350		2850	mV
AC Common-Mode Output Voltage, RMS			25	mV
Differential Output Voltage, Long Mode			845	mV
Differential Output Voltage, Short Mode			600	mV
Near-End Eye Height, Differential	70			mV
Far-End Eye Height, Differential	30			mV

Far-End Pre-cursor Ratio	-4.5		+2.5	%
Differential Termination Mismatch			10	%
Transition Time, 20% to 80%	9.5			ps
DC Common-Mode Output Voltage	-350		2850	mV

5、Transmitter Optical Characteristics — Per Lane

Parameter	Symbol	Min	Typ.	Max	Unit
Signaling Rate			53.125 ±100ppm		GBd
Modulation Format			PAM4		
Wavelength Range	λC	844	850	863	nm
RMS Spectral Width	Δλ			0.6	nm
Average Launch Power	PAVG	-4.6		+4.0	dBm
OMAouter, max(TECQ,TDECQ) ≤1.8dB	OMAouter	-2.6		+3.5	dBm
OMAouter, 1.8 < max(TECQ,TDECQ) ≤4.4dB	OMAouter	-4.4 + max(TECQ,TDECQ)		+3.5	dBm
Transmitter and Dispersion Eye Closure	TDECQ			4.4	dB
Transmitter Eye Closure	TECQ			4.4	dB
Extinction Ratio	ER	2.5			dB
Transmitter Power Excursion	TPE			2.3	dB
Transmitter Transition Time	Tt			17	ps
RIN14OMA[1]	RIN			-132	dB/Hz
Optical Return Loss Tolerance[1]	ORL			14	dB
Average Launch Power of OFF Transmitter	POFF			-30	dBm
Encircled Flux at 19μm		≥86%			
Encircled Flux at 4.5μm				≤30%	

6、Receiver Optical Characteristics — Per Lane

Parameter	Symbol	Min	Typ.	Max	Unit
Signaling Rate			53.125		GBd

			±100ppm		
Modulation Format			PAM4		
Receiver Wavelength Range	λR	842		948	nm
Damage Threshold	AOPD	+5.0			dBm
Average Receive Power	AOPR	-6.3		+4.0	dBm
Receive Power (OMAouter)	OMA-R			+3.5	dBm
Receiver Reflectance[2]	RR			-15	dB
Receiver Sensitivity (OMAouter)[3]	SEN			max(-4.4, TECQ - 6.2)	dBm
Stressed Receiver Sensitivity	SRS			-1.8	dBm

7、Stressed Receiver Test Conditions

Parameter	Value	Unit
Stressed Eye Closure for PAM4 (SECQ)	4.4	dB
OMAouter of Each Aggressor Lane	3.5	dBm
Pre-FEC BER	2.4×10^{-4}	

Recommended Host Board Power Supply Circuit

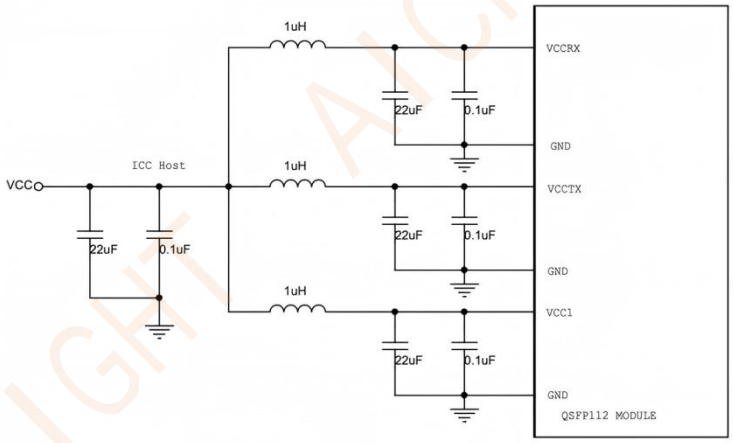


Figure 1: Recommended Host Board Power Supply Circuit

Recommended Interface Circuit

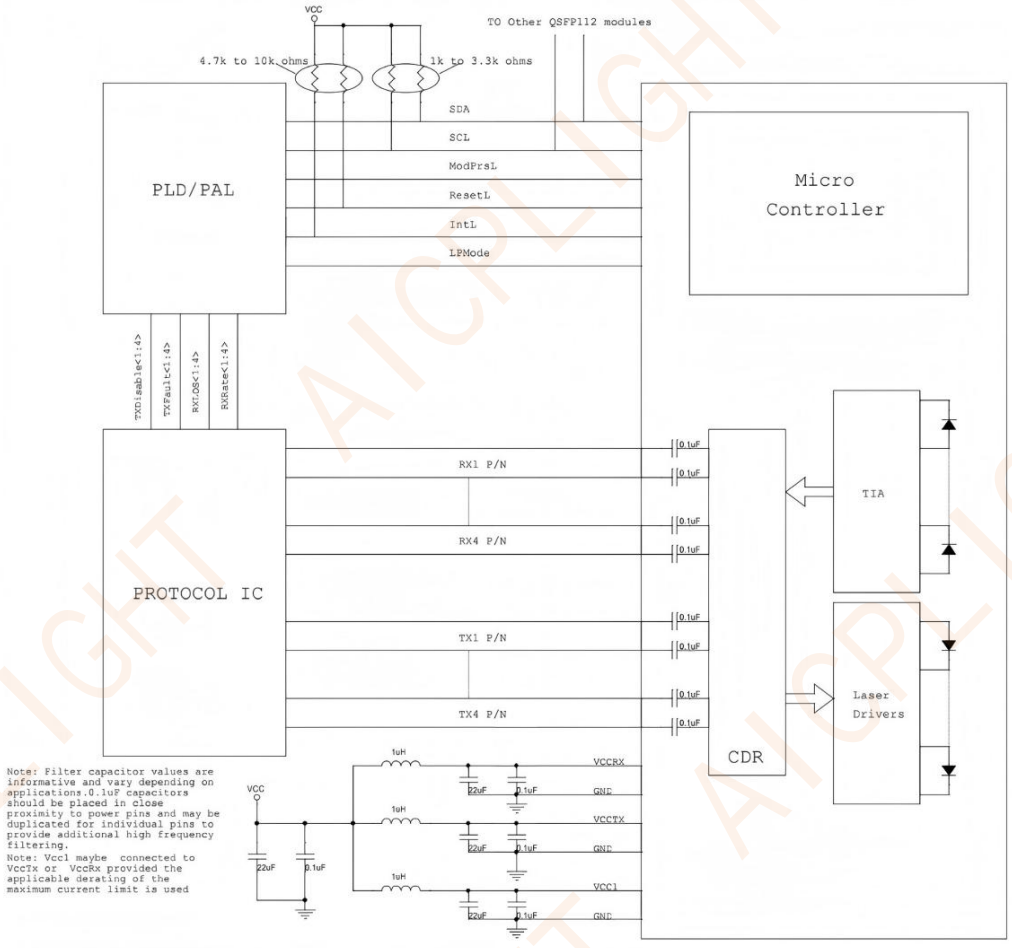


Figure2: Recommended Interface Circuit

Optical Interface

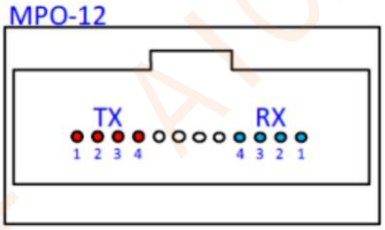


Figure3: Optical Lane Sequence

Pin-out Definition

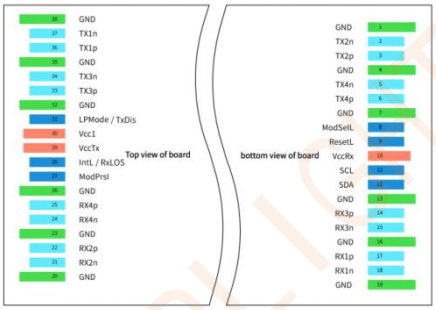


Figure4:QSFP112 Module contact assignment



Figure5: Pin view

Pin Function Definitions

PIN	Module contact	Logic	Symbol	Description	Note
1	1		GND	Ground	1
2			GND	Ground	1
3	2	CML-I	Tx2n	Transmitter Inverted Data Input	
4	3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
5	4		GND	Ground	1
6			GND	Ground	1
7	5	CML-I	Tx4n	Transmitter Inverted Data Input	
8	6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
9	7		GND	Ground	1
10			GND	Ground	1
11	8	LVTTL-I	ModSelL	Select	
12	9	LVTTL-1	ResetL	Reset	
13	10		Vcc Rx	+3.3V Power supply receiver	2
14			Vcc Rx	+3.3V Power supply receiver	2
15	11	LVCMOS-I/O	SCL	2-wire serial interface clock	
16	12	LVCMOS-I/O	SDA	2-wire serial interface data	
17	13		GND	Ground	1
18			GND	Ground	1
19	14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
20	15	CML-O	Rx3n	Receiver Inverted Data Output	
21	16		GND	Ground	1
22			GND	Ground	1
23	17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
24	18	CML-O	Rx1n	Receiver Inverted Data Output	
25	19		GND	Ground	1
26			GND	Ground	1
27	20		GND	Ground	1
28			GND	Ground	1
29	21	CML-O	Rx2n	Receiver Inverted Data Output	
30	22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
31	23		GND	Ground	1
32			GND	Ground	1
33	24	CML-O	Rx4n	Receiver Inverted Data Output	
34	25	CML-O	Rx4p	Receiver Non-Inverted Data Output	

35	26		GND	Ground	1
36			GND	Ground	1
37	27	LVTTL-O	ModPrsL	Present	
38	28	LVTTL-O	IntL/RxLOS	Interrupt/optional RxLOS	
39	29		Vcc Tx	+3.3V Power supply transmitter	2
40			Vcc Tx	+3.3V Power supply transmitter	2
41	30		$Vcc1_2$	+3.3V Power Supply	2
42	31	LVTTL-I	LPMode/TxD is	Low Power Mode/optional TX Disable	
43	32		GND	Ground	1
44			GND	Ground	1
45	33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
46	34	CML-I	Tx3n	Transmitter Inverted Data Input	
47	35		GND	Ground	1
48			GND	Ground	1
49	36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
50	37	CML-I	Tx1n	Transmitter Inverted Data Input	
51	38		GND	Ground	1
52			GND	Ground	1

Note1:GND is the symbol for signal and supply(power)common for the QSFP112module.Allare common within the QSFP112 module and all voltages are referenced to this potential unless otherwise noted.Connect these directly to the host board signal-common ground plane.

Note2: Vcc Rx,Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements,defined for the host side of the Host Edge Card Connector,are listed in Table 4.Recommended host board power supply fitering is shown in Figure 4.Vcc Rx,Vecc1and Vcc Tx may be intemally connected within the QSFP112 module in any combination.The connector pins are each rated for amaximum current of 1.5A(max.current of 2.0 Ais required for high module power of15-20W).

Monitoring Specification

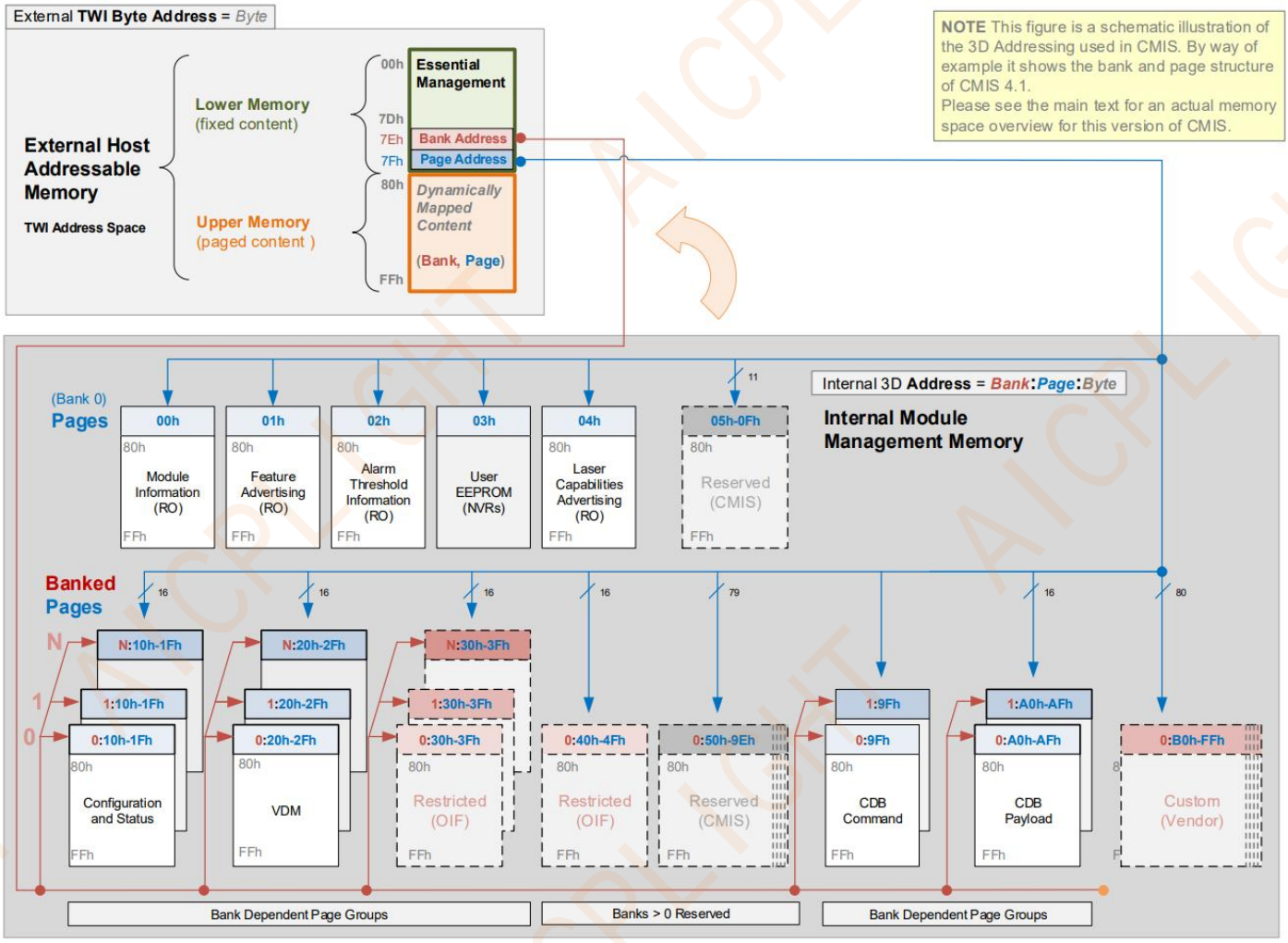


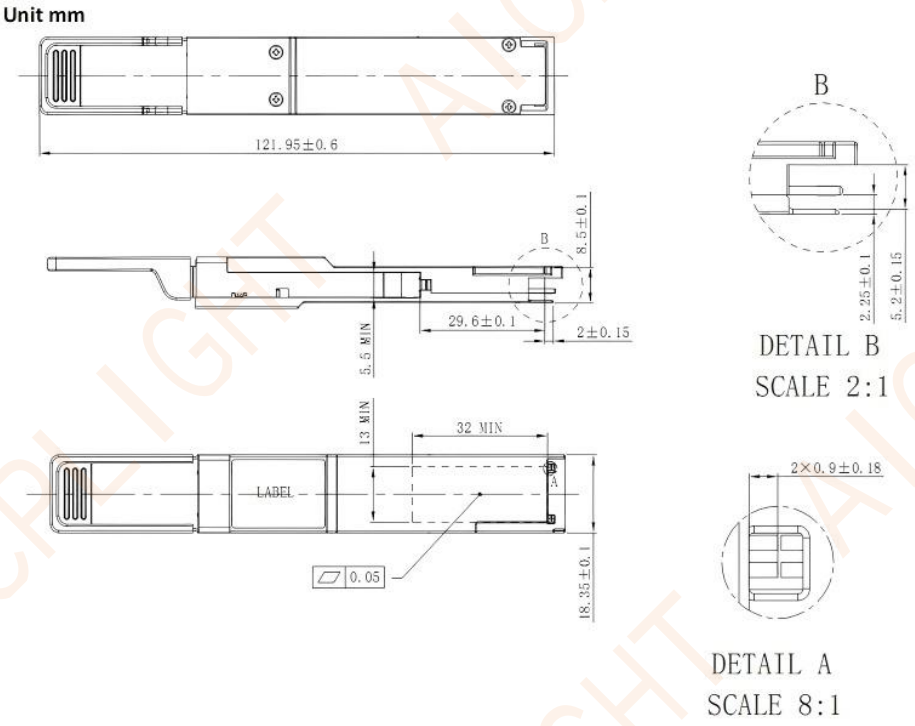
Figure5: Memory map

Memory map Table

Byte	Unit	Name	Description
Lower Page 00h			
0-2	3	Management Characteristics	Basic Information about how this module is managed
3	1	Global Status Information	Current state of Module, Interrupt signal status
4-7	4	Flag Summary	Summary of Flags set on specific Pages (and Banks)
8-13	6	Module-Level Flags	Flags that are not lane or Data Path specific
14-25	12	Module-Level Monitors	Monitors that are not lane or Data Path specific
26-30	5	Module-Level Controls	Controls applicable to the module as a whole
31-36	6	Module-Level Masks	Mask bits for the Module-Level Flags
37-38	2	CDB Command Status	Status of current CDB command
39-40	2	Module Active Firmware Version	Module Active Firmware Version number
41	1	Fault Information	Fault cause for entering ModuleFault state

42-63	22		Reserved
64-84	21		Custom
85-117	33	Supported Applications Advertising	Applications supported by module Data Path(s)
118-125	8	Password Facilities	Password Entry and Change (mechanism only)
126-127	2	Page Mapping	Page mapping into host addressable Upper Memory
Upper Page 00h			
128	1	SFF8024IdentifierCopy	Copy of Byte 00h:0
129-144	16	VendorName	Vendor name (ASCII)
145-147	3	Vendor OUI	Vendor IEEE company ID
148-163	16	Vendor PN	Part number provided by vendor (ASCII)
164-165	2	Vendor Rev	Revision level for part number provided by vendor (ASCII)
166-181	16	Vendor SN	Vendor Serial Number (ASCII)
182-189	8	DateCode	Manufacturing Date Code (ASCII)
190-199	10	CLEICode	Common Language Equipment Identification Code (ASCII)
200-201	2	ModulePowerCharacteristics	Module power characteristics
202	1	CableAssemblyLinkLength	Cable length (for cable assembly modules only)
203	1	ConnectorType	Connector type of the media interface
204-209	6	Copper Cable Attenuation	Attenuation characteristics (passive copper cables only)
210	1	MediaLaneInformation	Supported near end media lanes (all modules)
211	1	Cable Assembly Information	Far end modules information (cable assemblies only)
212	1	MediaInterfaceTechnology	Information on media side device or cable technology
213-220	8		Reserved
221	1		Custom
222	1	PageChecksum	Page Checksum over bytes 128-221
223-255	33		Custom

Mechanical Dimension



Handling and Safety Precautions：

- **ESD Protection:** Use proper electrostatic discharge (ESD) protection when handling, installing, or removing the module.
- **Installation and Removal:** Insert or remove the QSFP112 module using the pull tab or release mechanism. Do not force the module into the cage or pull on the fiber cable.
- **Thermal Management:** Ensure sufficient airflow and proper contact with the host-system heatsink. Do not obstruct the cooling path, as the module may become hot during operation.
- **Connector Cleaning:** Keep MTP/MPO or LC optical interfaces clean and protected with dust caps when not in use. Clean connector end faces before connection.
- **Fiber Handling:** Avoid excessive bending, pulling, twisting, or crushing of fiber cables. Follow the specified minimum bend radius.
- **Laser Safety:** Do not look directly into the optical port or connected fiber while the module is powered. Do not disassemble or modify the module.

Ordering Information

PN	Description
Q112-400G-SR4	400GBASE-SR4 QSFP112 PAM4 850nm 50m DOM MTP/MPO-12 APC MMF Optical Transceiver Module
Q112-400G-DR4	400GBASE-DR4 QSFP112 PAM4 1310nm 500m DOM MTP/MPO-12 APC SMF Optical Transceiver Module