Product Specification

400GBASE-DR4 QSFP-DD PAM4 1310nm 500m DOM MTP/MPO-12 APC SMF Optical Transceiver Module

PN: QDD-400G-DR4



Features

- Hot-pluggable QSFP-DD form factor
- Aggregate data rate of 425Gb/s
- 8 × 53.125Gb/s PAM4 host electrical lanes
- 4 × 106.25Gb/s PAM4 optical lanes
- Single +3.3V power supply
- MTP/MPO-12 APC connector
- Maximum power consumption ≤9.0W
- Transmission distance from 2m to 500m over single-mode fiber
- 4-channel 1310nm EML transmitter
- 4-channel PIN receiver array
- Built-in digital diagnostic monitoring
- Requires host-side RS(544,514) FEC
- Commercial case temperature range of 0°C to 70°C

Compliance

- QSFP-DD MSA
- CMIS 5.0 (Management Interface)
- IEEE 802.3bs (400GBASE-DR4 / 400GAUI-8)
- RoHS
- Class 1 Laser Product

Applications

- 400GBASE-DR4 Ethernet links
- 4×100GBASE-DR breakout links
- QSFP-DD switch and NIC ports
- Data center and HPC interconnects

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Description

The QDD-400G-DR4 is a hot-pluggable QSFP-DD optical transceiver designed for IEEE 802.3bs 400GBASE-DR4 Ethernet links over parallel single-mode fiber. The host-side electrical interface uses eight 53.125 Gb/s PAM4 lanes operating at 26.5625 GBd per lane, while the optical interface uses four 106.25 Gb/s PAM4 lanes operating at 53.125 GBd per lane. The module supports transmission distances from 2 meters up to 500 meters over SMF through an MTP/MPO-12 APC optical interface.

The optical transmitter uses four parallel 1310nm EML channels, while the receiver incorporates a four-channel PIN photodiode array. Eight active fibers within the MTP/MPO-12 interface provide four transmit and four receive optical lanes. Internal gearbox and retiming functions convert between the eight-lane 400GAUI-8 host interface and the four-lane optical interface.

The module operates from a single 3.3V power supply with a maximum power consumption of 9.0W and supports a commercial case temperature range of 0°C to 70°C. Digital diagnostic monitoring and module control are provided through the 2-wire management interface. Standard 400GBASE-DR4 operation requires host-side RS(544,514) FEC. The module can also support compatible 4×100GBASE-DR and 2×200GBASE-DR2 breakout configurations when supported by the host platform.

Product performance Specifications

1、Basic Product Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit
Storage Temperature	TS	-40		+85	°C
Supply Voltage	VCC	-0.5		+3.6	V
Relative Humidity	RH	5		85	%

2、Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit
Operating Case Temperature	TC	0		70	°C
Power Supply Voltage	VCC	3.135	3.3	3.465	V
Maximum Power Consumption	PD			9.0	W
Aggregate Data Rate	DR		425		Gb/s
Host Electrical Lanes			8		lanes
Host Bit Rate per Lane			53.125		Gb/s
Host Signaling Rate per Lane			26.5625 ±100ppm		GBd
Optical Lanes			4		lanes
Optical Bit Rate per Lane			106.25		Gb/s
Optical Signaling Rate per Lane			53.125 ±100ppm		GBd

Modulation Format			PAM4		
Link Distance over SMF	D	2		500	m
Pre-FEC Bit Error Ratio	BER			2.4×10^{-4}	
FEC			Host-side RS(544,514)		
Power-On Initialization Time	Tini			2000	ms

3、High-Speed Electrical Input Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit
Signaling Rate per Lane	TP1		26.5625 ±100ppm		GBd
Modulation Format			PAM4		
Differential Peak-to-Peak Input Voltage	TP1a			900	mVpp
Differential Termination Mismatch	TP1			10	%
Single-Ended Voltage Tolerance Range	TP1a	-0.4		3.3	V
DC Common-Mode Input Voltage	TP1	-350		2850	mV
Differential Input Return Loss	TP1		Per IEEE 802.3bs 400GAUI-8 requirements		dB
Differential-to-Common-Mode Conversion	TP1		Per IEEE 802.3bs 400GAUI-8 requirements		dB
Module Stressed Input Test	TP1a		Per IEEE 802.3bs Clause 120E requirements		

4、High-Speed Electrical Output Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit
Signaling Rate per Lane	TP4		26.5625 ±100ppm		GBd
Modulation Format			PAM4		
Differential Peak-to-Peak Output Voltage	TP4			900	mVpp
AC Common-Mode Output Voltage, RMS	TP4			17.5	mV
Differential Termination Mismatch	TP4			10	%

Differential Output Return Loss	TP4		Per IEEE 802.3bs 400GAUI-8 requirements		dB
Near-End Eye Symmetry Mask Width	TP4		0.265		UI
Near-End Eye Height, Differential	TP4	70			mV
Far-End Eye Symmetry Mask Width	TP4		0.20		UI
Far-End Eye Height, Differential	TP4	30			mV
Far-End Pre-cursor ISI Ratio	TP4	-4.5		+2.5	dB
Transition Time, 20% to 80%	TP4	9.5			ps
DC Common-Mode Output Voltage	TP4	-350		2850	mV

5、Transmitter Optical Characteristics — Per Lane

Parameter	Symbol	Min	Typ.	Max	Unit
Optical Signaling Rate			53.125 ±100ppm		GBd
Optical Bit Rate			106.25		Gb/s
Modulation Format			PAM4		
Wavelength Range	λC	1304.5	1310	1317.5	nm
Side-Mode Suppression Ratio	SMSR	30			dB
Average Launch Power	PAVG	-2.9		+4.0	dBm
Outer Optical Modulation Amplitude	OMAouter	-0.8		+4.2	dBm
Launch Power in OMAouter Minus TDECQ	OMAouter-TDECQ	-2.2			dBm
Transmitter and Dispersion Eye Closure for PAM4	TDECQ			3.4	dB
Extinction Ratio	ER	3.5			dB
Relative Intensity Noise	RIN21.4OMA			-136	dB/Hz
Optical Return Loss Tolerance	ORL			21.4	dB
Transmitter Reflectance				-26	dB
Average Launch Power of OFF Transmitter	POFF			-15	dBm

6、Receiver Optical Characteristics — Per Lane

Parameter	Symbol	Min	Typ.	Max	Unit
Optical Signaling Rate			53.125		GBd

			±100ppm		
Optical Bit Rate			106.25		Gb/s
Modulation Format			PAM4		
Wavelength Range	λR	1304.5	1310	1317.5	nm
Damage Threshold	THd	+5.0			dBm
Average Receive Power	RXPx	-5.9		+4.0	dBm
Receive Power (OMAouter)	RxOMAouter			+4.2	dBm
Receiver Reflectance	RR			-26	dB
Receiver Sensitivity (OMAouter)[1]	Rsens			max(-3.9, SECQ - 5.3)	dBm
Stressed Receiver Sensitivity (OMAouter)[2]	SRS			-1.9	dBm
LOS Assert[3]	LOSA	-15			dBm
LOS De-assert[3]	LOSD			-8.9	dBm
LOS Hysteresis[3]	LOSH	0.5			dB

7、Stressed Receiver Test Conditions

Parameter	Value	Unit
Stressed Eye Closure for PAM4 (SECQ)	3.4	dB
SECQ − $10\log_{10}$ (Ceq)	3.4	dB
OMAouter of Each Aggressor Lane	4.2	dBm
Pre-FEC BER	2.4×10^{-4}	
Test Pattern	PRBS31Q	

Note 1: Receiver sensitivity is an informative parameter. For the current IEEE Clause 124 specification, receiver sensitivity is defined as RS = max(-3.9, SECQ - 5.3) dBm. The normative receiver requirement is stressed receiver sensitivity.

Note 2: Stressed receiver sensitivity is measured using a 400GBASE-DR4 conformance test signal at TP3 at a pre-FEC BER of 2.4×10^{-4}.

Note 3: LOS thresholds are implementation-dependent and should be verified against the actual receiver specification before final release.

Note 4: Average launch power and average receive power minimum values are informative and are not the principal indicators of transmitter or receiver performance.

Note 5: Even when TDECQ is below 1.4dB, the minimum OMAouter must still meet the specified OMAouter minimum value.

Note 6: Standard 400GBASE-DR4 operation requires host-side RS(544,514) FEC.

Note 7: The host electrical interface uses eight 26.5625GBd PAM4 lanes, while the optical interface uses four 53.125GBd PAM4 lanes.

Recommended Host Board Power Supply Circuit

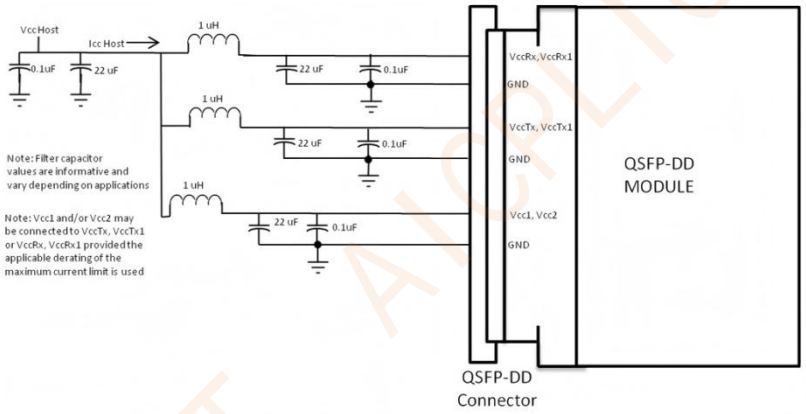


Figure 1: Recommended Host Board Power Supply Circuit

Recommended Interface Circuit

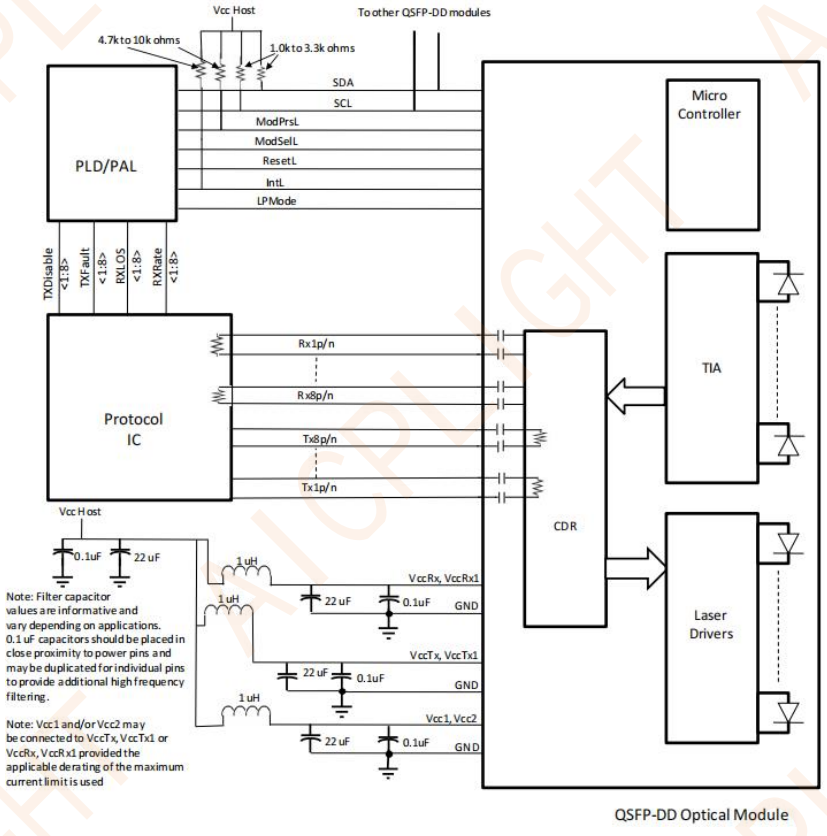


Figure2: Recommended Interface Circuit

Optical Interface

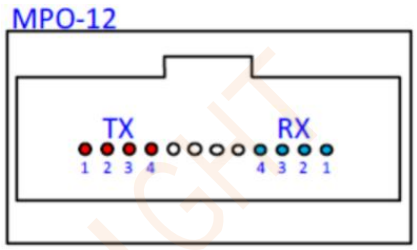


Figure3: Optical Lane Sequence

Pin-out Definition

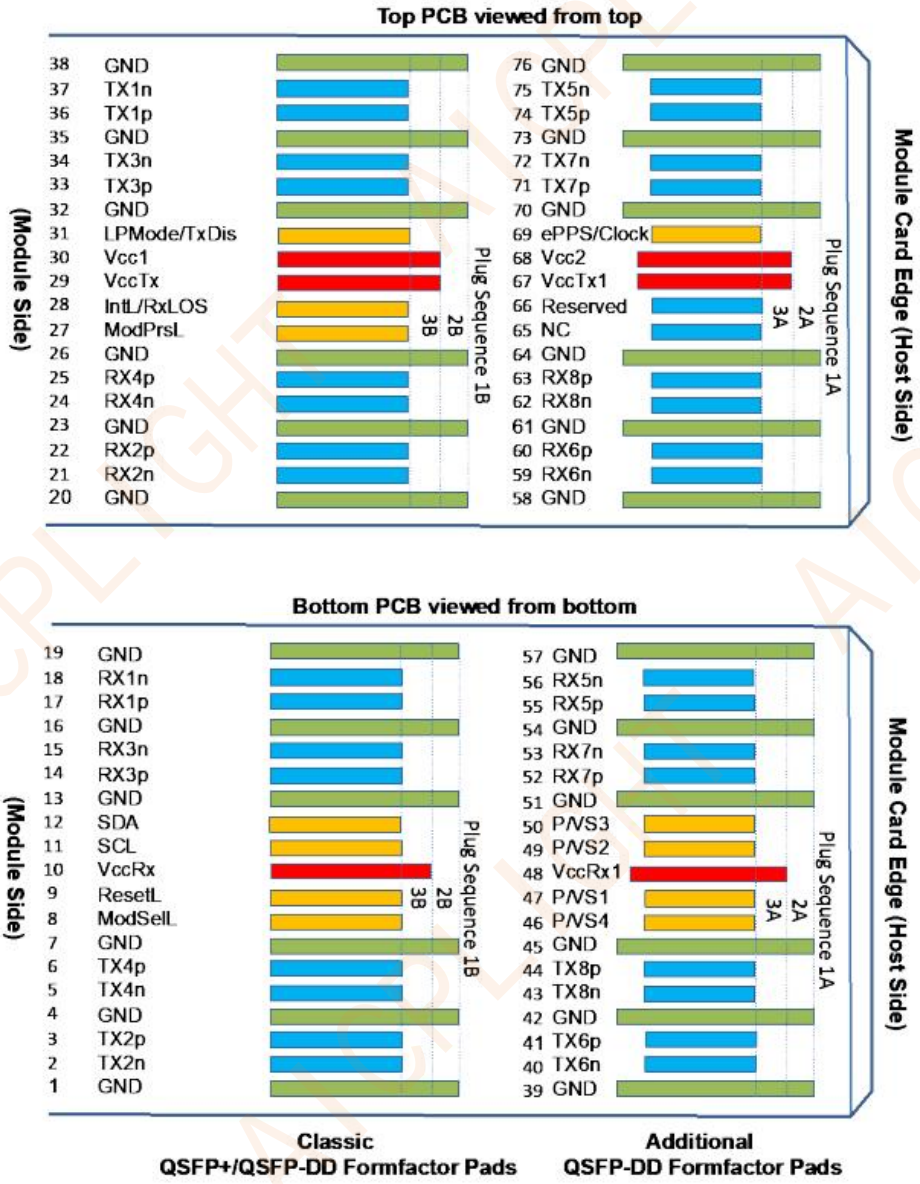


Figure4: Pin view

Pin Function Definitions

Pin	Logic	Symbol	Description	Plug Sequence 4	Note
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		Vcc Rx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	

12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL/RxLOSL	Interrupt. Optionally configurable as RxLOSL via the management interface (SFF-8636)	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46	LVCMOS/CML-I	P/VS4	Programmable/Module Vendor Specific 4	3A	5
47	LVCMOS/CML-I	I P/VS1	Programmable/Module Vendor Specific 1	3A	5
48		VccRx1	3.3V Power Supply	2A	2
49	LVCMOS/CML-O	P/VS2	Programmable/Module Vendor Specific 2	3A	5
50	LVCMOS/CML-O	P/VS3	Programmable/Module Vendor Specific 3	3A	5
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	

57		GND	Ground	1A	1
58		GND	Ground	3A	
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	1A	1
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future Use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVCMOS-I	ePPS/Clock	1PPS PTP clock or reference clock input	3A	6
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Note1:QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFPDD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane. Each connector Gnd contact is rated for a steady state current of 500 mA.

Note2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Supply requirements defined for the host side of the Host Card Edge Connector are listed in Table 13. For power classes 4 and above the module differential loading of input voltage pads must not result in exceeding contact current limits. Each connector Vcc contact is rated for a steady state current of 2000 mA.

Note3: Reserved pad recommended to be terminated with 10 kΩ to ground on the host. Pad 65 (No Connect) Shall be left unconnected within the module, optionally pad 65 may get terminated with 10 kΩ to ground on the host.

Note4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (See Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFPDD pads. Sequence 1A and 1B will then occur simultaneously, followed by 2A and 2B, followed by 3A and 3B.

Note5: Full definitions of the P/VSx signals currently under development. For module designs using programmable/vendor specific inputs P/VS1 and P/VS4 signals it is recommended each to be terminated in the module with 10 kΩ. For host designs using programmable/vendor specific outputs P/VS2 and P/VS3 signals it is recommended each to be terminated on the host with 10 kΩ.

Note6:for host not implementing ePPS/Clock, it is not necessary to parallel terminate the ePPS/Clock signal to ground on the host. ePPS/Clock already has parallel termination in the module see 4.2.6.

Monitoring Specification

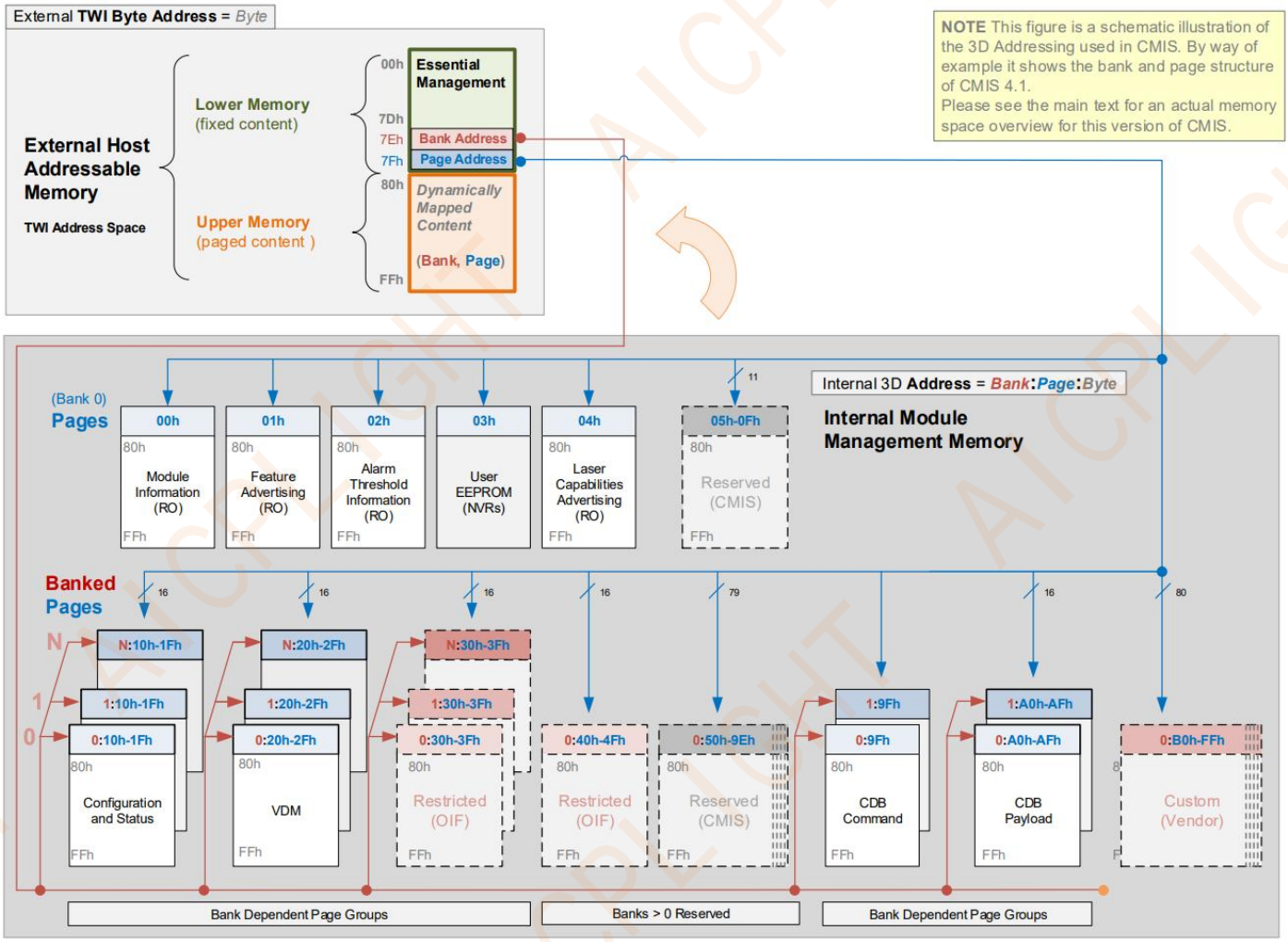


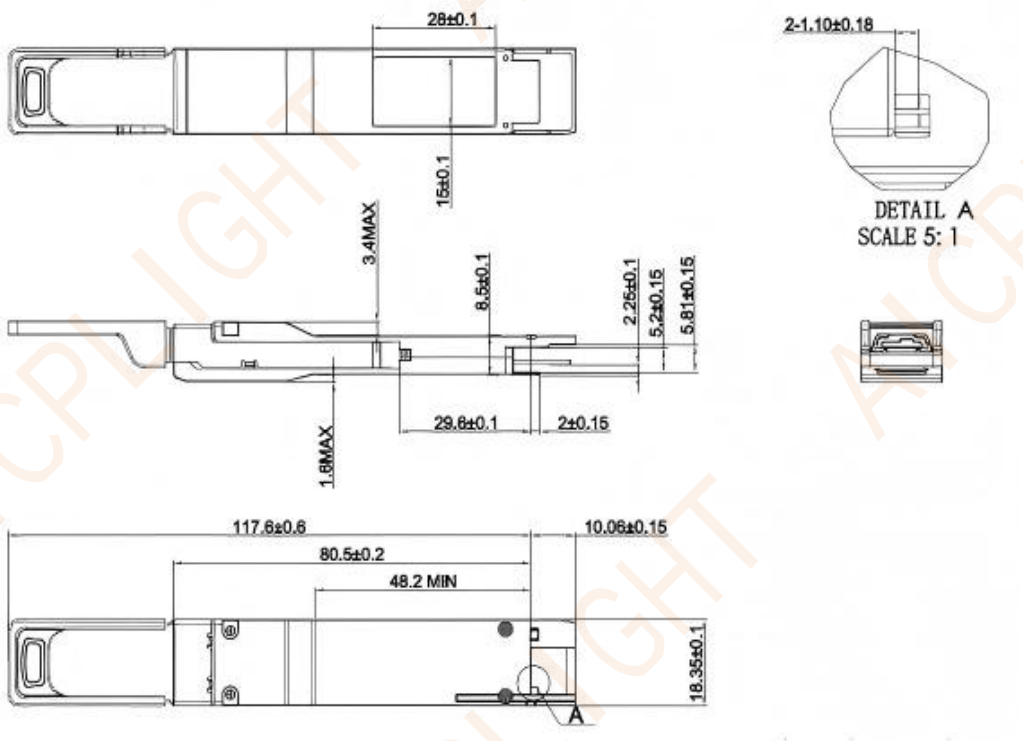
Figure5: Memory map

Memory map Table

Byte	Unit	Name	Description
Lower Page 00h			
0-2	3	Management Characteristics	Basic Information about how this module is managed
3	1	Global Status Information	Current state of Module, Interrupt signal status
4-7	4	Flag Summary	Summary of Flags set on specific Pages (and Banks)
8-13	6	Module-Level Flags	Flags that are not lane or Data Path specific
14-25	12	Module-Level Monitors	Monitors that are not lane or Data Path specific
26-30	5	Module-Level Controls	Controls applicable to the module as a whole
31-36	6	Module-Level Masks	Mask bits for the Module-Level Flags
37-38	2	CDB Command Status	Status of current CDB command
39-40	2	Module Active Firmware Version	Module Active Firmware Version number
41	1	Fault Information	Fault cause for entering ModuleFault state
42-63	22		Reserved

64-84	21		Custom
85-117	33	Supported Applications Advertising	Applications supported by module Data Path(s)
118-125	8	Password Facilities	Password Entry and Change (mechanism only)
126-127	2	Page Mapping	Page mapping into host addressable Upper Memory
Upper Page 00h			
128	1	SFF8024IdentifierCopy	Copy of Byte 00h:0
129-144	16	VendorName	Vendor name (ASCII)
145-147	3	Vendor OUI	Vendor IEEE company ID
148-163	16	Vendor PN	Part number provided by vendor (ASCII)
164-165	2	Vendor Rev	Revision level for part number provided by vendor (ASCII)
166-181	16	Vendor SN	Vendor Serial Number (ASCII)
182-189	8	DateCode	Manufacturing Date Code (ASCII)
190-199	10	CLEICode	Common Language Equipment Identification Code (ASCII)
200-201	2	ModulePowerCharacteristics	Module power characteristics
202	1	CableAssemblyLinkLength	Cable length (for cable assembly modules only)
203	1	ConnectorType	Connector type of the media interface
204-209	6	Copper Cable Attenuation	Attenuation characteristics (passive copper cables only)
210	1	MediaLaneInformation	Supported near end media lanes (all modules)
211	1	Cable Assembly Information	Far end modules information (cable assemblies only)
212	1	MediaInterfaceTechnology	Information on media side device or cable technology
213-220	8		Reserved
221	1		Custom
222	1	PageChecksum	Page Checksum over bytes 128-221
223-255	33		Custom

Mechanical Dimension



Handling and Safety Precautions：

- **ESD Protection:** Use proper electrostatic discharge (ESD) protection when handling, installing, or removing the module.
- **Installation and Removal:** Insert or remove the module using the pull tab or release mechanism. Do not force the module into the cage or pull on the fiber cable.
- **Thermal Management:** Ensure sufficient airflow and proper heatsink contact. The module may become hot during operation.
- **Connector Cleaning:** Keep MTP/MPO or LC optical interfaces clean and protected with dust caps when not in use. Clean connector end faces before connection.
- **Fiber Handling:** Avoid excessive bending, pulling, twisting, or crushing of fiber cables. Follow the specified minimum bend radius.
- **Laser Safety:** Do not look directly into the optical port or connected fiber while the module is powered. Do not disassemble or modify the module.

Ordering Information

PN	Description
QDD-400G-SR8	400GBASE-SR8 QSFP-DD PAM4 850nm 100m DOM MTP/MPO-16/APC MMF Optical Transceiver Module
QDD-400G-SR4	400GBASE-SR4 QSFP-DD PAM4 850nm 100m DOM MTP/MPO-12 APC MMF Optical Transceiver Module
QDD-400G-DR4	400GBASE-DR4 QSFP-DD PAM4 1310nm 500m DOM MTP/MPO-12 APC SMF Optical

	Transceiver Module
QDD-400G-FR4	400GBASE-FR4 QSFP-DD PAM4 1310nm 2km DOM Duplex LC/UPC SMF Optical Transceiver Module