Product Specification

100GBASE-SR4 QSFP28 850nm 100m DOM MTP/MPO-12 UPC MMF InfiniBand EDR Optical Transceiver Module

PN: QSFP-EDR-SR4



Features

- Hot-pluggable QSFP28 form factor
- Aggregate signaling rate of 103.125Gb/s
- 4 × 25.78125Gb/s NRZ electrical lanes
- Single +3.3V power supply
- MTP/MPO-12 UPC connector
- Maximum power consumption ≤2.0W
- Up to 70m over OM3 multimode fiber
- Up to 100m over OM4 multimode fiber
- 4-channel 850nm VCSEL transmitter array
- 4-channel PIN receiver array
- Built-in digital diagnostic monitoring
- Host-side Clause 91 RS-FEC for 100GBASE-SR4 Ethernet operation
- Supports 100Gb/s InfiniBand EDR applications
- Commercial case temperature range of 0°C to 70°C

Compliance

- QSFP28 MSA
- SFF-8636 (Management Interface)
- SFF-8665 (QSFP Pluggable Transceiver Solution)
- IEEE 802.3bm (100GBASE-SR4)

Applications

- 100Gb/s InfiniBand EDR links
- InfiniBand EDR switch-to-adapter interconnects
- InfiniBand EDR switch-to-switch interconnects
- 100GBASE-SR4 Ethernet links
- 4 × 25GBASE-SR breakout links
- QSFP28 switch and router connections
- Server and network adapter connections
- AI and HPC cluster interconnects
- High-density data center networks

Description

The QSFP-EDR-SR4 is a hot-pluggable QSFP28 optical transceiver designed for 100Gb/s InfiniBand EDR and Ethernet interconnects over parallel multimode fiber. It uses four independent NRZ electrical lanes operating at 25.78125Gb/s per lane, corresponding to an aggregate signaling rate of 103.125Gb/s. The module supports transmission distances of up to 70 meters over OM3 multimode fiber and 100 meters over OM4 multimode fiber through a single MTP/MPO-12 UPC optical interface.

The optical transmitter incorporates a four-channel 850nm VCSEL array, while the receiver uses a four-channel PIN photodiode array with transimpedance amplifiers. Eight active fibers within the MTP/MPO-12 interface provide four transmit and four receive optical channels. The module uses parallel optical transmission without wavelength multiplexing or demultiplexing, enabling high-bandwidth connectivity for compatible QSFP28 network adapters and switches.

The module operates from a single 3.3V power supply with a maximum power consumption of 2.0W and supports a commercial case temperature range of 0° C to 70° C. Digital diagnostic monitoring and module management are provided through the SFF-8636 two-wire management interface. For Ethernet applications, host-side Clause 91 RS-FEC is supported for 100GBASE-SR4 operation. For InfiniBand EDR deployments, protocol operation and platform compatibility must follow the applicable host system and InfiniBand implementation. The QSFP-EDR-SR4 is intended for InfiniBand EDR networks, data center interconnects, and high-performance computing (HPC) environments.

Product performance Specifications

1、Absolute Maximum Ratings

Parameter	Symbol	Min	Typ.	Max	Unit
Storage Temperature	TS	-40		+85	°C
Supply Voltage	VCC	0		3.6	V

2、Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit
Operating Case Temperature	TC	0		70	°C
Relative Humidity	RH	5		85	%
Power Supply Voltage	VCC	3.135	3.3	3.465	V
Power Dissipation	PD			2.0	W
Aggregate Data Rate	DR		103.125		Gb/s
Signaling Rate per Lane			25.78125 ±100ppm		Gb/s
Maximum Link Distance on OM3				70	m
Maximum Link Distance on OM4				100	m
FEC Requirement			Clause 91 RS-FEC		

3、High-Speed Electrical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit
Input Differential Impedance	ZIN		100		Ω
Output Differential Impedance	ZOUT		100		Ω
Differential Data Input Swing	VIN,pp	180		700	mVpp
Differential Data Output Swing	VOUT,pp			900	mVpp
Differential Data Output Eye Width	EW	0.57			UI
Differential Data Output Eye Height	EH	228			mV
Differential Data Output Vertical Eye Closure	VEC			5.5	dB

4、Transmitter Optical Characteristics — Per Lane

Parameter	Symbol	Min	Typ.	Max	Unit
Signaling Rate			25.78125 ±100ppm		Gb/s
Center Wavelength	λC	840	850	860	nm
RMS Spectral Width				0.6	nm
Average Launch Power	PAVG	-8.4		+2.4	dBm

Optical Modulation Amplitude	OMA	-6.4		+3.0	dBm
Launch Power in OMA Minus TDEC	OMA-TDEC	-7.3			dBm
Transmitter and Dispersion Eye Closure	TDEC			4.3	dB
Extinction Ratio	ER	2.0			dB
Optical Return Loss Tolerance	ORL			12	dB
Average Launch Power of OFF Transmitter	POFF			-30	dBm

5、100GBASE-SR4 Transmitter Eye Mask

Parameter	Value
Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}	{0.30, 0.38, 0.45, 0.35, 0.41, 0.50}
Hit Ratio	1.5×10^{-3} hits per sample

6、Receiver Optical Characteristics — Per Lane

Parameter	Symbol	Min	Typ.	Max	Unit
Signaling Rate			25.78125 ±100ppm		Gb/s
Receiver Wavelength Range	λR	840		860	nm
Damage Threshold	THd	+3.4			dBm
Average Receive Power	PAVG	-10.3		+2.4	dBm
Receive Power (OMA)	RxOMA			+3.0	dBm
Stressed Receiver Sensitivity (OMA)[1]	SRS			-5.2	dBm
Receiver Reflectance				-12	dB
LOS Assert	LOSA	-30			dBm

7、Stressed Receiver Test Conditions

Parameter	Value	Unit
Stressed Eye Closure (SEC)	4.3	dB
Stressed Eye J2 Jitter	0.39	UI
Stressed Eye J4 Jitter	0.53	UI
OMA of Each Aggressor Lane	3.0	dBm
Stressed Receiver Eye Mask {X1, X2, X3, Y1, Y2, Y3}	{0.28, 0.50, 0.50, 0.33, 0.33, 0.40}	

Eye Mask Hit Ratio	5×10^{-5}	hits per sample

Note1: Stressed receiver sensitivity is measured using a 100GBASE-SR4 conformance test signal at TP3 at BER < 5×10^{-5}.

Note2:LOS thresholds are implementation-dependent and should be verified against the actual receiver specification.

Note2: Average receive power per lane is an informative operating parameter and is not the principal measure of receiver sensitivity.

Note2: Optical transmitter and receiver specifications are defined per lane at a nominal signaling rate of 25.78125 Gb/s.

Recommended Host Board Power Supply Circuit

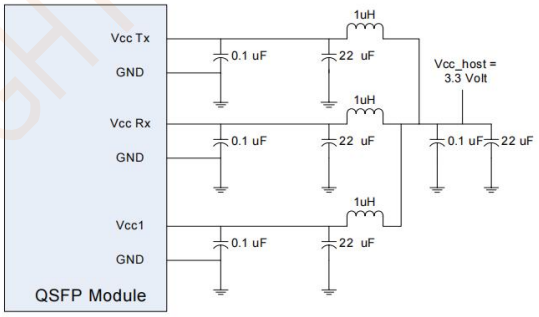


Figure 1: Recommended Host Board Power Supply Circuit

Recommended Interface Circuit

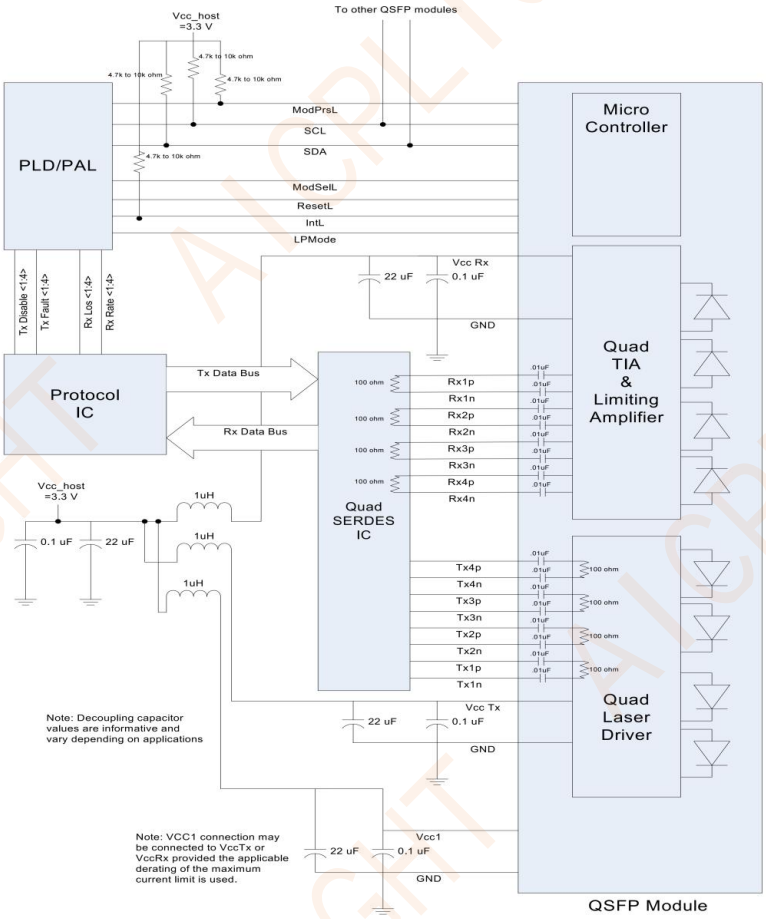


Figure2: Recommended Interface Circuit

Optical Interface

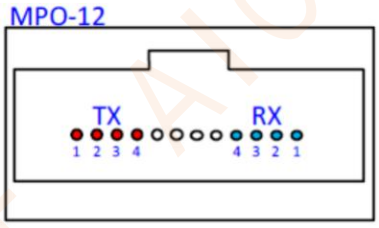


Figure3:Optical Lane Sequence

Pin-out Definition

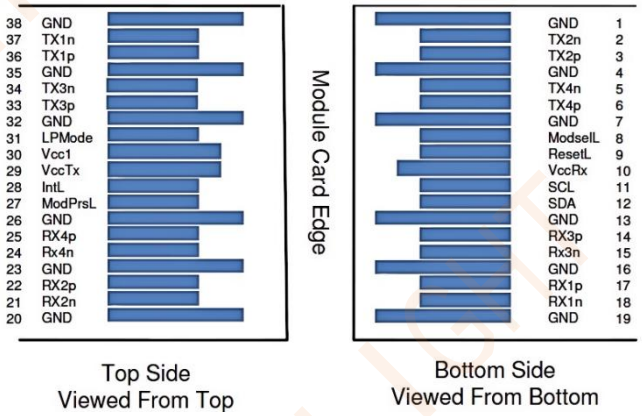


Figure4:Pin view

Pin Function Definitions

Pin	Logic	Symbol	Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	4
9	LVTTL-I	ReSelL	Module Select	4
10		Vcc Rx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	4
12	LVCMOS-I/O	SDA	2-wire serial interface data	4
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3

15	CML-O	Rx3n	Receiver Inverted Data Output	3
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3
18	CML-O	Rx1n	Receiver Inverted Data Output	3
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3
25	CML-O	Rx4p	Receiver Non-Inverted Data Output Ground	3
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	4
28	LVTTL-O	IntL	Interrupt	4
29		Vcc Tx	+3.3V Power supply transmitter	2
30		Vcc1	+3.3V Power supply	2
31	LVTTL-I	LPMode	Low Power Mode	4
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3
34	CML-I	Tx3n	Transmitter Inverted Data Input	3
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3
37	CML-I	Tx1n	Transmitter Inverted Data Input	3
38		GND	Ground	1

Note1:GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table. Recommended host board power supply filtering is shown in Host board power supply circuit. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP module in any combination. The connector pins are each rated for a maximum current of 500 mA.

Note3: High-speed signal interfaces require differential pairs (e.g. TX1+/TX1-) with tightly matched impedances (typically 100Ω).

Note4: The management and control signals are based on LVTTL level logic and are used for functions such as module selection and reset.

Monitoring Specification

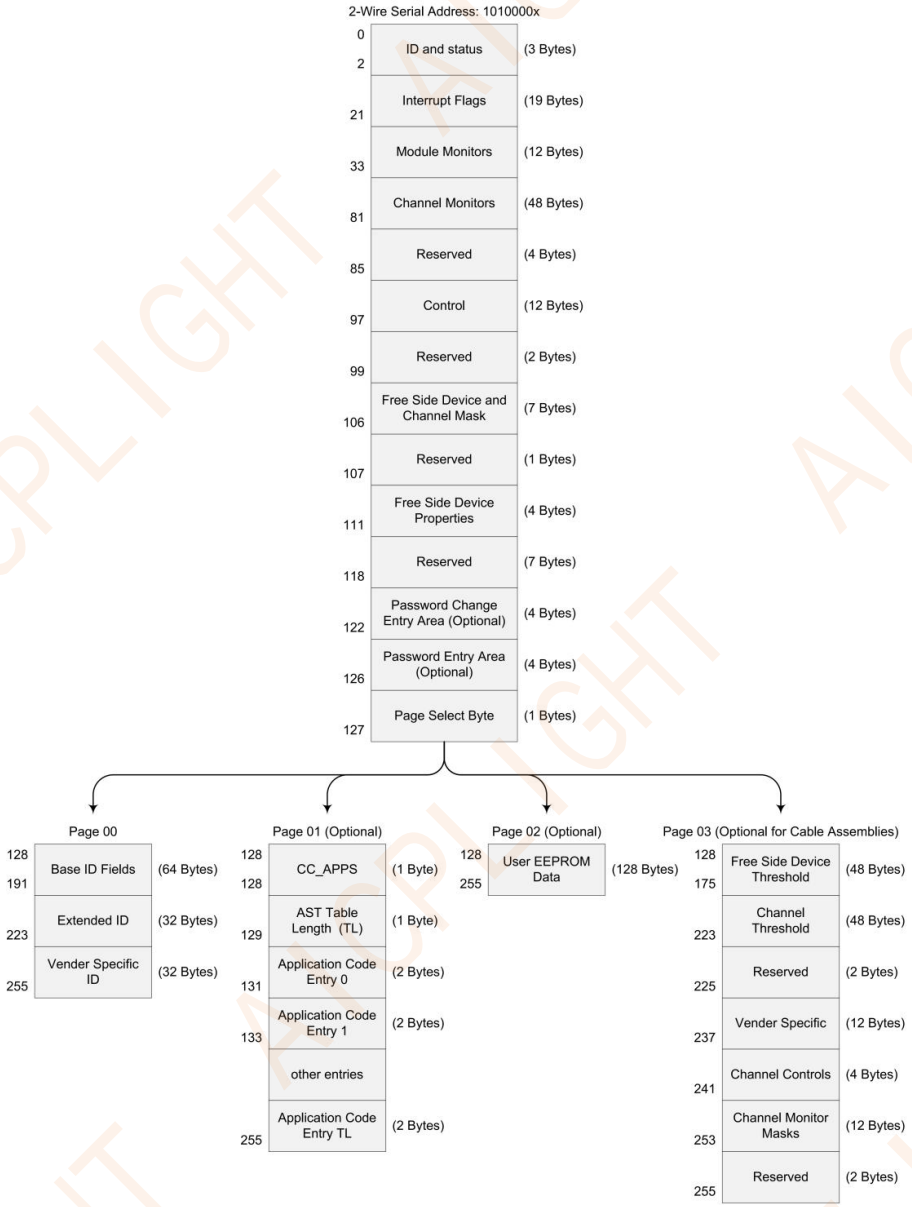


Figure5: Memory map

Memory map Table

Byte	Unit	Name	Description
			Lower Page 00h
0	1	Identifier	Type of transceiver,Page 00h Byte 0 and Page 00h Byte 128 shall contain the same parameter values.
1	1	Status	Revision Compliance
2	1	Status	Status indicators

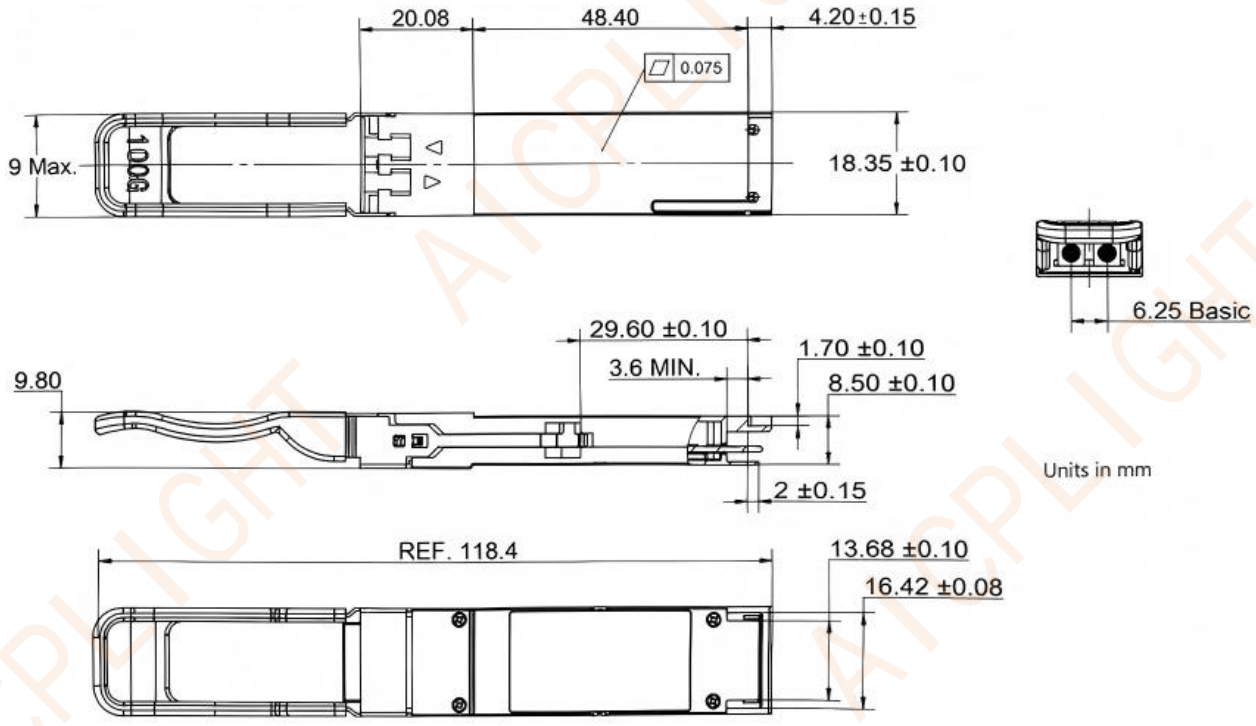
3-21	19	Interrupt Flags	Consist of interrupt flags for LOS, Tx Fault, warnings and alarms. The non-asserted state shall be 0b.
22	1	Temperature MSB	Internally measured temperature (MSB)
23	1	Temperature LSB	Internally measured temperature (LSB)
24-25	2	Reserved	Reserved
26	1	Supply Voltage MSB	Internally measured supply voltage (MSB)
27	1	Supply Voltage LSB	Internally measured supply voltage (LSB)
28-29	2	Reserved	Reserved
30-33	4	Vendor Specific	Vendor Specific
34	1	Rx1 Power MSB	Internally measured Rx1 input power
35	1	Rx1 Power LSB	
36	1	Rx2 Power MSB	Internally measured Rx2 input power
37	1	Rx2 Power LSB	
38	1	Rx3 Power MSB	Internally measured Rx3 input power
39	1	Rx3 Power LSB	
40	1	Rx4 Power MSB	Internally measured Rx4 input power
41	1	Rx4 Power LSB	
42	1	Tx1 Bias MSB	Internally measured Tx1 bias
43	1	Tx1 Bias LSB	
44	1	Tx2 Bias MSB	Internally measured Tx2 bias
45	1	Tx2 Bias LSB	
46	1	Tx3 Bias MSB	Internally measured Tx3 bias
47	1	Tx3 Bias LSB	
48	1	Tx4 Bias MSB	Internally measured Tx4 bias
49	1	Tx4 Bias LSB	
50	1	Tx1 Power MSB	Internally measured Tx1 Power
51	1	Tx1 Power LSB	
52	1	Tx2 Power MSB	Internally measured Tx2 Power
53	1	Tx2 Power LSB	
54	1	Tx3 Power MSB	Internally measured Tx3 Power
55	1	Tx3 Power LSB	
56	1	Tx4 Power MSB	Internally measured Tx4 Power
57	1	Tx4 Power LSB	
58-65	8	Reserved	Reserved channel monitor set 4
66-73	8	Reserved	Reserved channel monitor set 5
74-81	8	Vendor Specific	Vendor Specific
82-85	4	Reserved	Reserved
86-99	14	Control	Control
100-106	7	Free Side Device and Channel Masks	Free Side Device and Channel Masks
107-110	4	Free Side Device Properties	Free Side Device Properties

111-112	2	Assigned for use by PCI Express	Used for: - The PCI Express External Cable Specification - The PCI Express OCuLink Specification
113-117	4	Free Side Device Properties	Free Side Device Properties
118	1	Reserved	Reserved
119-122	4	Password Change Entry Area	Password Change Entry Area
123-126	4	Password Entry Area	Password Entry Area
127	1	Page Select Byte	Page Select Byte
Upper Page 00h			
128	1	Identifier	Identifier Type of free side device.(See SFF-8024 Transceiver Management)
129	1	Ext. Identifier	Extended Identifier of free side device. Includes power classes, CLEI codes, CDR capability.
130	1	Connector Type	Code for media connector type. (See SFF-8024 Transceiver Management)
131-138	8	Specification Compliance	Code for electronic or optical compatibility.
139	1	Encoding	Code for serial encoding algorithm. (See SFF-8024 Transceiver Management)
140	1	Signaling rate, nominal	Nominal signaling rate, units of 100 MBd. For rate > 25.4 GBd, set this to FFh and use Byte 222.
141	1	Extended Rate Select Compliance	Tags for extended rate select compliance.
142	1	Length (SMF)	Link length supported at the signaling rate in byte 140 or page 00h byte 222, for SMF fiber in km *. A value of 1 shall be used for reaches from 0 to 1 km.
143	1	Length (OM3 50 um)	Link length supported at the signaling rate in byte 140 or page 00h byte 222, for EBW 50/125 um fiber (OM3), units of 2 m *
144	1	Length (OM2 50 um)	Link length supported at the signaling rate in byte 140 or page 00h byte 222, for 50/125 um fiber (OM2), units of 1 m *
145	1	Length (OM1 62.5 um) or Copper Cable Attenuation	Link length supported at the signaling rate in byte 140 or page 00h byte 222, for 62.5/125 um fiber (OM1), units of 1 m *, or copper cable attenuation in dB at 25.78 GHz.
146	1	Length (passive copper or active cable or OM4 50 um)	Length of passive or active cable assembly (units of 1 m) or link length supported at the signaling rate in byte 140 or page 00h byte 222, for OM4 50/125 um fiber (units of 2 m) as indicated by Byte 147. See 6.3.12.
147	1	Device technology	Device technology
148-163	16	Vendor name	Free side device vendor name (ASCII)
164	1	Extended Module	Extended Module codes for InfiniBand.
165-167	3	Vendor OUI	Free side device vendor IEEE company ID.
168-183	16	Vendor PN	Part number provided by free side device vendor(ASCII)
184-185	2	Vendor rev	Revision level for part number provided by the vendor(ASCII)

186-187	2	Wavelength or Copper Cable Attenuation	Nominal laser wavelength (wavelength=value/20 in nm) or copper cable attenuation in dB at 2.5 GHz (Byte 186) and 5.0 GHz (Byte 187)
188-189	2	Wavelength tolerance or Copper Cable Attenuation	The range of laser wavelength (+/- value) from nominal wavelength. (wavelength Tol. =value/200 in nm) or copper cable attenuation in dB at 7.0 GHz (Byte 188) and 12.9 GHz (Byte 189)
190	1	Max case temp	Maximum case temperature
191	1	CC_BASE	Check code for base ID fields (Bytes 128-190)
192	1	Link codes	Extended Specification Compliance Codes (See SFF-8024)
193-195	3	Options	Optional features implemented.
196-211	16	Vendor SN	Serial number provided by vendor.(ASCII)
212-219	8	Date Code	Vendor's manufacturing date code.
220	1	Diagnostic Monitoring Type	Indicates which type of diagnostic monitoring is implemented (if any) in the free side device. Bit 1,0 Reserved.
221	1	Enhanced Options	Indicates which optional enhanced features are implemented in the free side device.
222	1	CC_EXT	Check code for the Extended ID Fields (Bytes 192-222)
224-255	32	Vendor Specific	Vendor Specific EEPROM
Page 02h (Optional)			
128-255	128	User EEPROM Data	
Page 03h (Optional)			
128-129	2	Temp High Alarm	MSB at lower byte address
130-131	2	Temp Low Alarm	MSB at lower byte address
132-133	2	Temp High Warning	MSB at lower byte address
134-135	2	Temp Low Warning	MSB at lower byte address
136-143	8	Reserved	Reserved
144-145	2	Vcc High Alarm	MSB at lower byte address
146-147	2	Vcc Low Alarm	MSB at lower byte address
148-149	2	Vcc High Warning	MSB at lower byte address
150-151	2	Vcc Low Warning	MSB at lower byte address
152-159	8	Reserved	Reserved
160-175	16	Vendor Specific	Vendor Specific
176-177	2	Rx Power High Alarm	MSB at lower byte address
178-179	2	Rx Power Low Alarm	MSB at lower byte address
180-181	2	Rx Power High Warning	MSB at lower byte address
182-183	2	Rx Power Low Warning	MSB at lower byte address
184-185	2	Tx Bias High Alarm	MSB at lower byte address
186-187	2	Tx Bias Low Alarm	MSB at lower byte address
188-189	2	Tx Bias High Warning	MSB at lower byte address
190-191	2	Tx Bias Low Warning	MSB at lower byte address
192-193	2	Tx Power High Alarm	MSB at lower byte address
194-195	2	Tx Power Low Alarm	MSB at lower byte address
196-197	2	Tx Power High Warning	MSB at lower byte address

198-199	2	Tx Power Low Warning	MSB at lower byte address
200-207	8	Reserved	Reserved thresholds for channel parameter set 4
208-215	8	Reserved	Reserved thresholds for channel parameter set 5
216-223	8	Vendor Specific	Vendor Specific
224	1	Tx EQ & Rx Emphasis Magnitude ID	Tx EQ & Rx Emphasis Magnitude ID
225	1	Rx output amplitude support indicators	Rx output amplitude support indicators
226-229	4	Control options advertising	Control options advertising
230-241	12	Optional Channel Controls	Optional Channel Controls
242-247	6	Channel Monitor Masks	Channel Monitor Masks
248-249	2	Reserved	Reserved channel monitor masks set 4
250-251	2	Reserved	Reserved channel monitor masks set 5
252-255	4	Reserved	Reserved

Mechanical Dimension



Handling and Safety Precautions:

- **ESD Precautions:** Follow standard electrostatic discharge (ESD) handling procedures when handling, installing, or removing the module. Use a grounded wrist strap or other appropriate ESD protection.
- **Hot-Plug Handling:** The QSFP+ module is hot-pluggable. Insert or remove the module only by holding the module housing and using the pull tab or release mechanism as intended.

- **Optical Connector Protection:** Keep the optical interface clean and protected from dust, moisture, oil, and other contaminants. Keep the dust cap installed whenever the optical connector is not in use.
- **Connector Cleaning:** Inspect and clean the MTP/MPO or LC connector end faces before connection. Do not touch the optical end faces directly with fingers or unapproved materials.
- **Fiber Cable Handling:** Avoid excessive bending, pulling, twisting, crushing, or other mechanical stress on the fiber cable. Follow the minimum bend-radius requirements specified for the fiber assembly.
- **Installation and Removal:** Ensure the module is correctly aligned with the QSFP+ cage before insertion. Do not force the module into the port or remove it without releasing the latch or pull tab.
- **Optical and Laser Safety:** Do not look directly into the optical port or the end of a connected fiber while the module is powered. Avoid direct eye exposure to emitted optical radiation.
- **Mechanical Handling:** Do not drop, crush, strike, or apply excessive mechanical force to the module, optical receptacle, housing, or pull tab.
- **Operating Environment:** Do not operate the module outside the specified temperature, humidity, supply-voltage, or power limits. Ensure sufficient airflow around the module during operation.
- **Disassembly:** Do not disassemble, modify, or attempt to repair the module. Opening the module may damage the optical and electronic components and affect product performance.

Ordering Information

PN	Description
QSFP-EDR-SR4	100GBASE-SR4 QSFP28 850nm 100m DOM MTP/MPO-12 UPC MMF InfiniBand EDR Optical Transceiver Module