Product Specification

1~50m 400G OSFP Flat Top to 400G QSFP-DD Active Optical Cable

PN:O400-QDD-A



Features

- Hot-pluggable OSFP Flat Top and QSFP-DD form factors
- 400G Ethernet connectivity
- 425Gb/s aggregate line bit rate
- 4×100G PAM4, 400GAUI-4-L C2M at the OSFP end
- 8×50G PAM4, 400GAUI-8 C2M at the QSFP-DD end
- Integrated retiming and lane-rate conversion
- 850nm VCSEL and PIN arrays
- Available lengths from 1m to 50m
- Single +3.3V power supply at each end
- Maximum power consumption ≤10W at the OSFP end
- Maximum power consumption ≤8W at the QSFP-DD end
- Digital diagnostic monitoring
- Operating case temperature range of 0°C to +70°C

Compliance

- OSFP MSA
- QSFP-DD MSA
- IEEE 802.3bs (400GAUI-8 C2M)
- IEEE 802.3ck (400GAUI-4-L C2M)
- CMIS 5.0
- RoHS compliant

Applications

- 400G Ethernet
- Data center networking
- AI and HPC clusters
- Cloud data centers
- OSFP-to-QSFP-DD switch and NIC links

Description

The O400-QDD-A is a 400G active optical cable designed to connect an OSFP Flat Top port to a QSFP-DD port. The QSFP-DD end uses an 8×50G PAM4 400GAUI-8 C2M electrical interface, while the OSFP Flat Top end uses a 4×100G PAM4 400GAUI-4-L C2M electrical interface.

Integrated retiming and lane-rate conversion provide 400GbE connectivity between the two different host electrical interfaces. The internal optical link uses four 100G-class PAM4 optical lanes with 850nm VCSEL transmitters, PIN receivers, and multimode fiber. The cable is available in lengths from 1m to 50m.

The integrated AOC assembly eliminates separate optical transceivers and external fiber patch cords. Both ends are hot-pluggable and support CMIS-based management and digital diagnostic monitoring. The O400-QDD-A is designed for 400GbE switch-to-switch and switch-to-NIC interconnects in data centers, AI clusters, and high-performance computing systems.

Product Performance Specifications

1、Absolute Maximum Ratings

Parameter	Symbol	Min	Typ.	Max	Unit
Storage Temperature	T_S	-40	—	+85	°C
Supply Voltage	V_CC	-0.3	—	3.6	V
Relative Humidity	RH	5	—	85	%

2、Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit
Operating Case Temperature	T_C	0	—	+70	°C
Power Supply Voltage	V_CC	3.135	3.3	3.465	V
Aggregate Line Bit Rate	DR	—	425	—	Gb/s
Cable Length	L	1	—	50	m
Pre-FEC Bit Error Ratio	BER	—	—	2.4×10^{-4}	—

3、Power Supply and Electrical Specifications

Parameter	Symbol	Min	Typ.	Max	Unit
Power Consumption — QSFP-DD End	P_D	—	—	8.0	W

Supply Current — QSFP-DD End	I_CC	—	—	2.55	A
Power Consumption — OSFP End	P_D	—	—	10.0	W
Supply Current — OSFP End	I_CC	—	—	3.19	A

4、Host Electrical Interface

Parameter	QSFP-DD End	OSFP Flat Top End
Host Electrical Interface	400GAUI-8 C2M	400GAUI-4-L C2M
Electrical Lane Count	8 TX + 8 RX	4 TX + 4 RX
Line Bit Rate per Lane	53.125Gb/s	106.25Gb/s
Signaling Rate per Lane	26.5625GBd ±100ppm	53.125GBd ±100ppm
Modulation Format	PAM4	PAM4
Aggregate Line Bit Rate	425Gb/s	425Gb/s
Lane-Rate Conversion	8×50G ↔ 4×100G	4×100G ↔ 8×50G

5、Transmitter Electrical Characteristics

Parameter	Interface	Test Point	Min.	Typ.	Max.	Unit
Signaling Rate per Lane	QSFP-DD / 400GAUI-8	TP1	—	26.5625 ±100ppm	—	GBd
Differential Peak-to-Peak Input Voltage Tolerance	QSFP-DD / 400GAUI-8	TP1a	900	—	—	mV
Differential Termination Mismatch	QSFP-DD / 400GAUI-8	TP1	—	—	10	%
Single-Ended Voltage Tolerance Range	QSFP-DD / 400GAUI-8	TP1a	-0.4	—	3.3	V
DC Common-Mode Voltage	QSFP-DD / 400GAUI-8	TP1	-350	—	2850	mV
Module Stressed Input Test	QSFP-DD / 400GAUI-8	TP1a	—	IEEE 802.3 Annex 120E	—	—
Signaling Rate per Lane	OSFP / 400GAUI-4-L	TP1	—	53.125 ±100ppm	—	GBd
Differential Peak-to-Peak Input Voltage Tolerance	OSFP / 400GAUI-4-L	TP1a	750	—	—	mV
Effective Input Return Loss	OSFP / 400GAUI-4-L	TP1	8.5	—	—	dB
Differential Termination Mismatch	OSFP / 400GAUI-4-L	TP1	—	—	10	%

Single-Ended Voltage Tolerance Range	OSFP / 400GAUI-4-L	TP1a	-0.4	—	3.3	V
DC Common-Mode Voltage	OSFP / 400GAUI-4-L	TP1	-350	—	2850	mV
Module Stressed Input Test	OSFP / 400GAUI-4-L	TP1a	—	IEEE 802.3ck 120G.3.4.3	—	—

6、Receiver Electrical Characteristics

Parameter	Interface	Test Point	Min.	Typ.	Max.	Unit
Signaling Rate per Lane	QSFP-DD / 400GAUI-8	TP4	—	26.5625 ±100ppm	—	GBd
AC Common-Mode Output Voltage, RMS	QSFP-DD / 400GAUI-8	TP4	—	—	17.5	mV
Differential Peak-to-Peak Output Voltage	QSFP-DD / 400GAUI-8	TP4	—	—	900	mV
Near-End Eye Symmetry Mask Width	QSFP-DD / 400GAUI-8	TP4	0.265	—	—	UI
Near-End Eye Height	QSFP-DD / 400GAUI-8	TP4	70	—	—	mV
Far-End Eye Symmetry Mask Width	QSFP-DD / 400GAUI-8	TP4	0.20	—	—	UI
Far-End Eye Height	QSFP-DD / 400GAUI-8	TP4	30	—	—	mV
Far-End Pre-Cursor ISI Ratio	QSFP-DD / 400GAUI-8	TP4	-4.5	—	+2.5	%
Differential Termination Mismatch	QSFP-DD / 400GAUI-8	TP4	—	—	10	%
Transition Time (20%–80%)	QSFP-DD / 400GAUI-8	TP4	9.5	—	—	ps
DC Common-Mode Voltage	QSFP-DD / 400GAUI-8	TP4	-350	—	2850	mV
Signaling Rate per Lane	OSFP / 400GAUI-4-L	TP4	—	53.125 ±100ppm	—	GBd
Differential Peak-to-Peak Output Voltage — Short Mode	OSFP / 400GAUI-4-L	TP4	—	—	600	mV
Differential Peak-to-Peak Output Voltage — Long Mode	OSFP / 400GAUI-4-L	TP4	—	—	845	mV
Eye Height	OSFP / 400GAUI-4-L	TP4	15	—	—	mV
Vertical Eye Closure	OSFP / 400GAUI-4-L	TP4	—	—	12	dB

Effective Output Return Loss	OSFP / 400GAUI-4-L	TP4	8.5	—	—	dB
Differential Termination Mismatch	OSFP / 400GAUI-4-L	TP4	—	—	10	%
Transition Time (20%–80%)	OSFP / 400GAUI-4-L	TP4	8.5	—	—	ps
DC Common-Mode Voltage	OSFP / 400GAUI-4-L	TP4	-350	—	2850	mV

7、Transmitter Optical Characteristics — Per Lane (OSFP Optical Engine)

Parameter	Symbol	Min	Typ.	Max	Unit
Optical Lane Count	—	—	4	—	lanes
Signaling Rate per Lane	SR	—	53.125 ±100ppm	—	GBd
Optical Bit Rate per Lane	BR	—	106.25	—	Gb/s
Modulation Format	—	—	PAM4	—	—
Center Wavelength	λ_C	842	850	948	nm
RMS Spectral Width	Δλ_RMS	—	—	0.65	nm
Average Launch Power per Lane	P_AVG	-4.6	—	+4.0	dBm
OMAouter per Lane	OMA_OUTER	-2.6	—	+3.5	dBm
TDECQ	TDECQ	—	—	4.4	dB
Extinction Ratio	ER	2.5	—	—	dB
Transmitter Power Excursion	TPE	—	—	2.3	dB
Average Launch Power of OFF Transmitter	P_OFF	—	—	-30	dBm
RIN14OMA	RIN	—	—	-132	dB/Hz
Optical Return Loss Tolerance	ORL	—	—	14	dB
Signaling Rate per Lane	SR	—	53.125 ±100ppm	—	GBd
Optical Bit Rate per Lane	BR	—	106.25	—	Gb/s

8、Receiver Optical Characteristics — Per Lane (OSFP Optical Engine)

Parameter	Symbol	Min	Typ.	Max	Unit
Optical Lane Count	—	—	4	—	lanes
Signaling Rate per Lane	SR	—	53.125	—	GBd

			±100ppm		
Modulation Format	—	—	PAM4	—	—
Receiver Wavelength Range	λ_R	842	—	948	nm
Damage Threshold	TH_D	+5.0	—	—	dBm
Average Receive Power per Lane	P_RX	-6.3	—	+4.0	dBm
Receive Power (OMAouter)	RX_OMA	—	—	+3.5	dBm
Receiver Reflectance	R_R	—	—	-15	dB
Stressed Receiver Sensitivity (OMAouter)	SRS	—	—	-1.8	dBm

9、Transmitter Optical Characteristics — Per Lane (QSFP-DD Optical Engine)

Parameter	Symbol	Min	Typ.	Max	Unit
Optical Lane Count	—	—	4	—	lanes
Signaling Rate per Lane	SR	—	53.125 ±100ppm	—	GBd
Optical Bit Rate per Lane	BR	—	106.25	—	Gb/s
Modulation Format	—	—	PAM4	—	—
Center Wavelength	λ_C	842	850	948	nm
RMS Spectral Width	Δλ_RMS	—	—	0.65	nm
Average Launch Power per Lane	P_AVG	-4.6	—	+4.0	dBm
OMAouter per Lane	OMA_OUTER	-2.6	—	+3.5	dBm
TDECQ	TDECQ	—	—	4.4	dB
Extinction Ratio	ER	2.5	—	—	dB
Transmitter Power Excursion	TPE	—	—	2.3	dB
Average Launch Power of OFF Transmitter	P_OFF	—	—	-30	dBm
RIN14OMA	RIN	—	—	-132	dB/Hz
Optical Return Loss Tolerance	ORL	—	—	14	dB

10、Receiver Optical Characteristics — Per Lane (QSFP-DD Optical Engine)

Parameter	Symbol	Min	Typ.	Max	Unit
Optical Lane Count	—	—	4	—	lanes
Signaling Rate per Lane	SR	—	53.125	—	GBd

			±100ppm		
Modulation Format	—	—	PAM4	—	—
Receiver Wavelength Range	λ_R	842	—	948	nm
Damage Threshold	TH_D	+5.0	—	—	dBm
Average Receive Power per Lane	P_RX	-6.3	—	+4.0	dBm
Receive Power (OMAouter)	RX_OMA	—	—	+3.5	dBm
Receiver Reflectance	R_R	—	—	-15	dB
Stressed Receiver Sensitivity (OMAouter)	SRS	—	—	-1.8	dBm

11、Encircled Flux Requirements

Parameter	Requirement
Encircled Flux at 19μm	≥86%
Encircled Flux at 4.5μm	≤30%

12、FEC and BER Specifications

Parameter	Symbol	Specification
Pre-FEC Bit Error Ratio	BER	$\leq 2.4 \times 10^{-4}$
FEC	—	Host-side RS-FEC
Modulation Format	—	PAM4
Optical Test Pattern	—	PRBS31Q

13、Management Interface Specifications

Parameter	Value
Management Interface	CMIS 5.0
Management Communication	2-wire serial interface
OSFP Management	CMIS
QSFP-DD Management	CMIS
Digital Diagnostic Monitoring	Supported
Module Identification	Supported

Module Status Monitoring	Supported

14、Cable and Mechanical Characteristics

Parameter	Specification
Cable Type	Active Optical Cable (AOC)
End A	OSFP Flat Top
End B	QSFP-DD
Internal Fiber Type	Multimode Fiber (MMF)
Internal Optical Architecture	4×100G PAM4 parallel optics
Transmitter Type	850nm VCSEL Array
Receiver Type	PIN Photodiode Array
Available Cable Length	1–50m
Electrical Conversion	4×100G PAM4 ↔ 8×50G PAM4
Hot-Pluggable	Yes

15、Environmental and Regulatory Specifications

Parameter	Specification
Operating Case Temperature	0°C to +70°C
Storage Temperature	-40°C to +85°C
Relative Humidity	5% to 85%, non-condensing
Supply Voltage	+3.3V nominal at each end
RoHS	Compliant

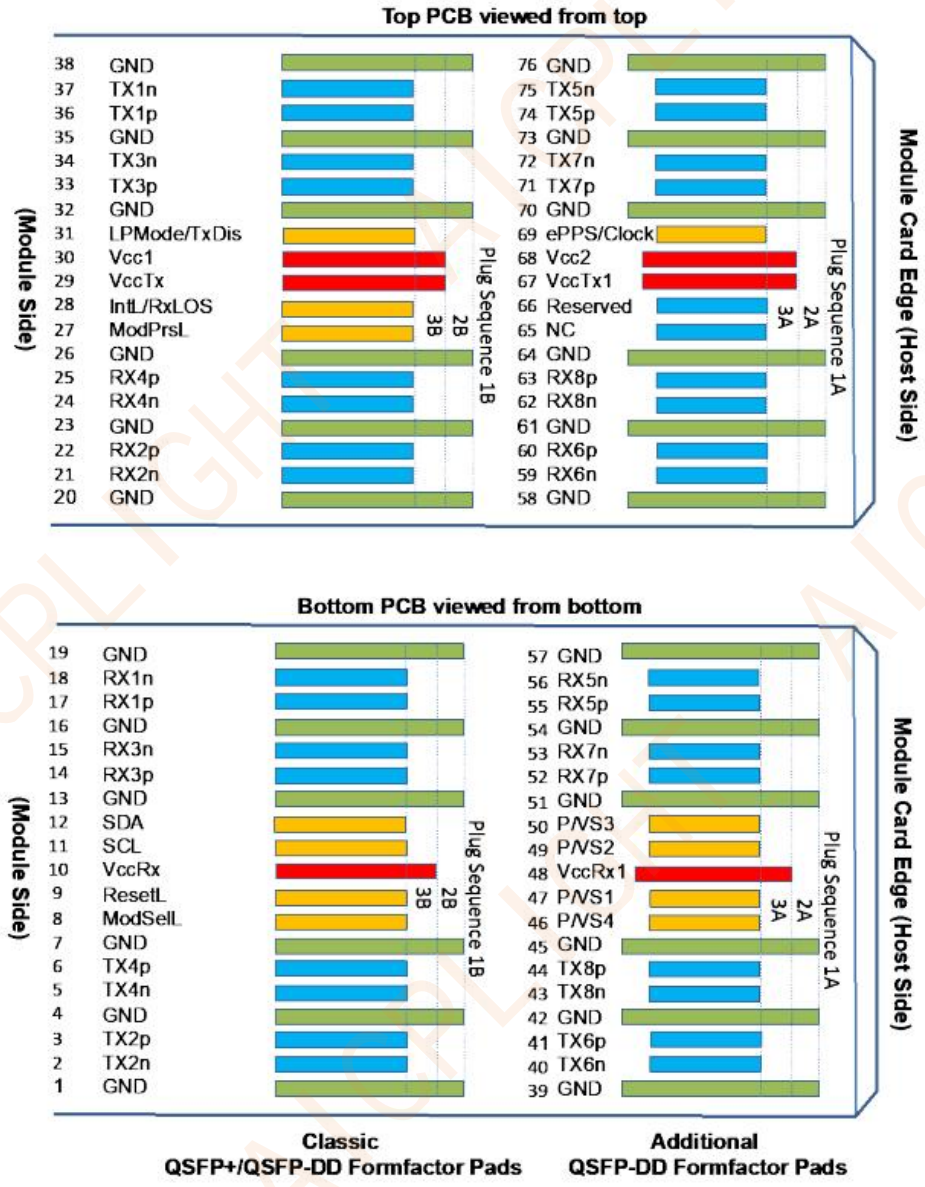


Figure3:Pin view(QSFP-DD)

Pin Function Definitions(QSFP-DD)

Pin	Logic	Symbol	Description	Plug Sequence 4	Note
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		Vcc Rx	+3.3V Power Supply Receiver	2B	2

11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL/RxLOSL	Interrupt. Optionally configurable as RxLOSL via the management interface (SFF-8636)	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46	LVCMOS/CML-I	P/VS4	Programmable/Module Vendor Specific 4	3A	5
47	LVCMOS/CML-I	I P/VS1	Programmable/Module Vendor Specific 1	3A	5
48		VccRx1	3.3V Power Supply	2A	2
49	LVCMOS/CML-O	P/VS2	Programmable/Module Vendor Specific 2	3A	5
50	LVCMOS/CML-O	P/VS3	Programmable/Module Vendor Specific 3	3A	5
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	

53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	3A	
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	1A	1
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future Use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVCMOS-I	ePPS/Clock	1PPS PTP clock or reference clock input	3A	6
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Note1:QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFPDD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane. Each connector Gnd contact is rated for a steady state current of 500 mA.

Note2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Supply requirements defined for the host side of the Host Card Edge Connector are listed in Table 13. For power classes 4 and above the module differential loading of input voltage pads must not result in exceeding contact current limits. Each connector Vcc contact is rated for a steady state current of 2000 mA.

Note3: Reserved pad recommended to be terminated with 10 kΩ to ground on the host. Pad 65 (No Connect) Shall be left unconnected within the module, optionally pad 65 may get terminated with 10 kΩ to ground on the host.

Note4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (See Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFPDD pads. Sequence 1A and 1B will then occur simultaneously, followed by 2A and 2B, followed by 3A and 3B.

Note5: Full definitions of the P/VSx signals currently under development. For module designs using programmable/vendor specific inputs P/VS1 and P/VS4 signals it is recommended each to be terminated in the module with 10 kΩ. For host designs using programmable/vendor specific outputs P/VS2 and P/VS3 signals it is recommended each to be terminated on the host with 10 kΩ.

Note6:for host not implementing ePPS/Clock, it is not necessary to parallel terminate the ePPS/Clock signal to ground on the host. ePPS/Clock already has parallel termination in the module see 4.2.6.

Pin-out Definition(OSFP)

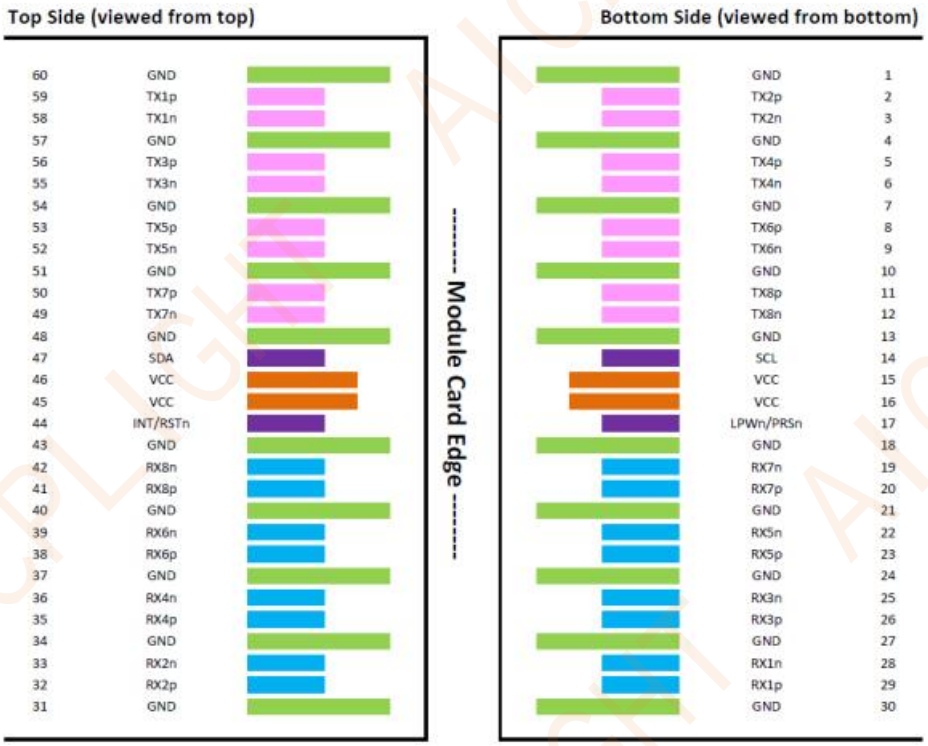


Figure4:Pin view(OSFP)

Pin Function Definitions(OSFP)

Pin	Logic	Symbol	Description	Note
1		GND	Ground	
2	CML-I	TX2p	Transmitter Data Non-Inverted	
3	CML-I	TX2n	Transmitter Data Inverted	
4		GND	Ground	
5	CML-I	TX4p	Transmitter Data Non-Inverted	
6	CML-I	TX4n	Transmitter Data Inverted	
7		GND	Ground	
8	CML-I	TX6p	Transmitter Data Non-Inverted	
9	CML-I	TX6n	Transmitter Data Inverted	
10		GND	Ground	
11	CML-I	TX8p	Transmitter Data Non-Inverted	
12	CML-I	TX8n	Transmitter Data Inverted	
13		GND	Ground	
14	LVCMOS-I/O	SCL	2-wire Serial interface clock	1
15		VCC	+3.3V Power	
16		VCC	+3.3V Power	

17	Multi-Level	LPWn/PRSn	Low-Power Mode / Module Present	2
18		GND	Ground	
19	CML-O	RX7n	Receiver Data Inverted	
20	CML-O	RX7p	Receiver Data Non-Inverted	
21		GND	Ground	
22	CML-O	RX5n	Receiver Data Inverted	
23	CML-O	RX5p	Receiver Data Non-Inverted	
24		GND	Ground	
25	CML-O	RX3n	Receiver Data Inverted	
26	CML-O	RX3p	Receiver Data Non-Inverted	
27		GND	Ground	
28	CML-O	RX1n	Receiver Data Inverted	
29	CML-O	RX1p	Receiver Data Non-Inverted	
30		GND	Ground	
31		GND	Ground	
32	CML-O	RX2p	Receiver Data Non-Inverted	
33	CML-O	RX2n	Receiver Data Inverted	
34		GND	Ground	
35	CML-O	RX4p	Receiver Data Non-Inverted	
36	CML-O	RX4n	Receiver Data Inverted	
37		GND	Ground	
38	CML-O	RX6p	Receiver Data Non-Inverted	
39	CML-O	RX6n	Receiver Data Inverted	
40		GND	Ground	
41	CML-O	RX8p	Receiver Data Non-Inverted	
42	CML-O	RX8n	Receiver Data Inverted	
43		GND	Ground	
44	Multi-Level	INT/RSTn	Module Interrupt / Module Reset	2
45		VCC	+3.3V Power	
46		VCC	+3.3V Power	
47	LVCMOS-I/O	SDA	2-wire Serial interface data	1
48		GND	Ground	
49	CML-I	TX7n	Transmitter Data Inverted	
50	CML-I	TX7p	Transmitter Data Non-Inverted	
51		GND	Ground	
52	CML-I	TX5n	Transmitter Data Inverted	
53	CML-I	TX5p	Transmitter Data Non-Inverted	
54		GND	Ground	
55	CML-I	TX3n	Transmitter Data Inverted	
56	CML-I	TX3p	Transmitter Data Non-Inverted	

57		GND	Ground	
58	CML-I	TX1n	Transmitter Data Inverted	
59	CML-I	TX1p	Transmitter Data Non-Inverted	
60		GND	Ground	

Note1: Open-Drain with pull up resistor on Host.

Note2: See pin description for required circuit.

Monitoring Specification

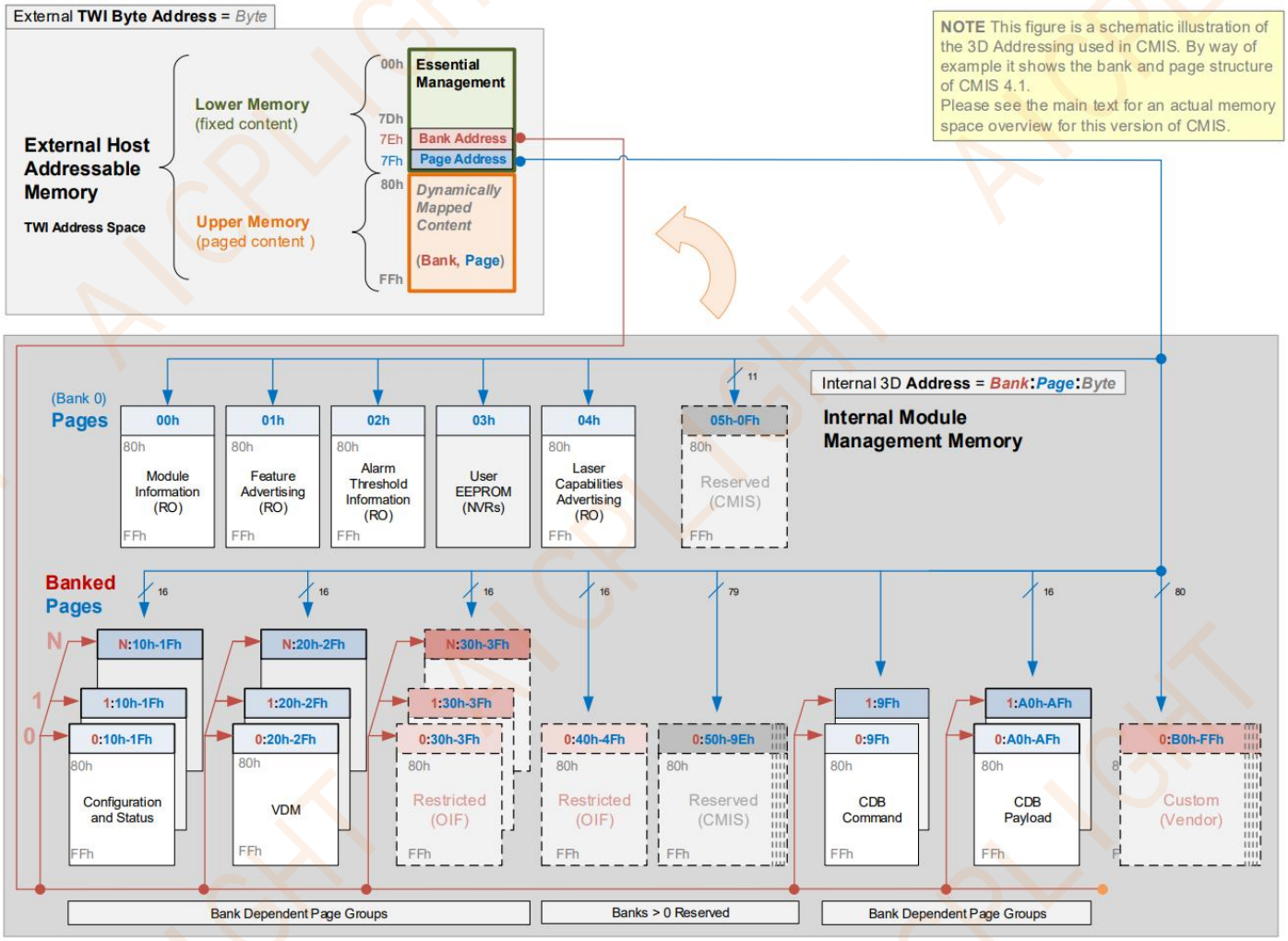
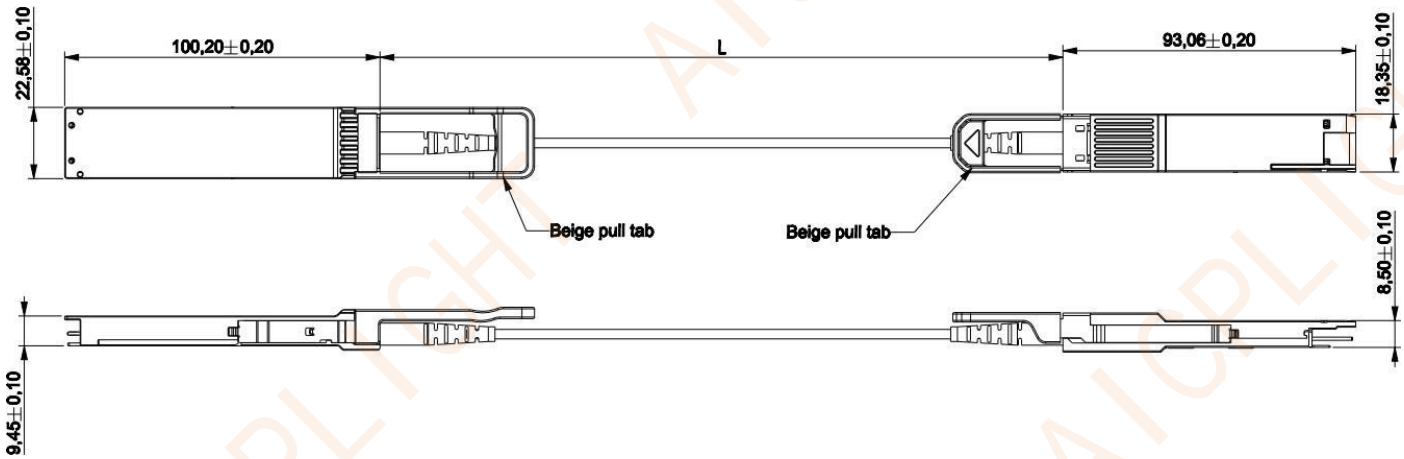


Figure5: Memory map

Memory map Table

Byte	Unit	Name	Description
		Lower Page 00h	
0-2	3	Management Characteristics	Basic Information about how this module is managed
3	1	Global Status Information	Current state of Module, Interrupt signal status
4-7	4	Flag Summary	Summary of Flags set on specific Pages (and Banks)
8-13	6	Module-Level Flags	Flags that are not lane or Data Path specific
14-25	12	Module-Level Monitors	Monitors that are not lane or Data Path specific
26-30	5	Module-Level Controls	Controls applicable to the module as a whole
31-36	6	Module-Level Masks	Mask bits for the Module-Level Flags
37-38	2	CDB Command Status	Status of current CDB command
39-40	2	Module Active Firmware Version	Module Active Firmware Version number
41	1	Fault Information	Fault cause for entering ModuleFault state
42-63	22		Reserved
64-84	21		Custom
85-117	33	Supported Applications Advertising	Applications supported by module Data Path(s)
118-125	8	Password Facilities	Password Entry and Change (mechanism only)
126-127	2	Page Mapping	Page mapping into host addressable Upper Memory
		Upper Page 00h	
128	1	SFF8024IdentifierCopy	Copy of Byte 00h:0
129-144	16	VendorName	Vendor name (ASCII)
145-147	3	Vendor OUI	Vendor IEEE company ID
148-163	16	Vendor PN	Part number provided by vendor (ASCII)
164-165	2	Vendor Rev	Revision level for part number provided by vendor (ASCII)
166-181	16	Vendor SN	Vendor Serial Number (ASCII)
182-189	8	DateCode	Manufacturing Date Code (ASCII)
190-199	10	CLEICode	Common Language Equipment Identification Code (ASCII)
200-201	2	ModulePowerCharacteristics	Module power characteristics
202	1	CableAssemblyLinkLength	Cable length (for cable assembly modules only)
203	1	ConnectorType	Connector type of the media interface
204-209	6	Copper Cable Attenuation	Attenuation characteristics (passive copper cables only)
210	1	MediaLaneInformation	Supported near end media lanes (all modules)
211	1	Cable Assembly Information	Far end modules information (cable assemblies only)
212	1	MediaInterfaceTechnology	Information on media side device or cable technology
213-220	8		Reserved
221	1		Custom
222	1	PageChecksum	Page Checksum over bytes 128-221
223-255	33		Custom

Mechanical Dimension



Note:

Diameter: 3mm

- Minimum bend radius:30 mm
- Cable color:Aqua
- When L≤1m, the tolerance is +70/-0 mm
- When 1 m<L<7 m, the tolerance is +100/-0 mm
- When L≥7 m,the tolerance is +2%L/-0

Handling and Safety Precautions:

- ESD Precautions: Follow standard ESD handling procedures when handling or installing the AOC.
- Bend Radius: Do not bend the cable below the specified minimum bend radius of 30 mm.
- Cable Handling: Avoid excessive pulling, twisting, crushing, or other mechanical stress on the cable.
- Installation and Removal: Use the pull tab or release mechanism when removing the AOC. Do not pull directly on the cable.
- Connector Protection: Keep the electrical connector contacts clean and protected from dust and contamination when not installed.
- Optical and Laser Safety: The optical fibers and optical engines are permanently integrated within the AOC assembly. Do not disassemble, modify, or attempt to service the internal optical components.

Ordering Information

PN	Description

Note: Other cable lengths from 1m to 50m are available upon request.