Product Specification

0.5~2.5m 400G OSFP Flat Top to 400G QSFP-DD
Passive Direct Attach Copper Twinax Cable

PN:O400-QDD-C



Features

- Supports 400G Ethernet connectivity
- 8 × 53.125 Gb/s PAM4 electrical lanes
- Wire gauge: 26 AWG, 28 AWG and 30 AWG
- Available in 1–3 m lengths
- Passive shielded twinax copper cable design
- Hot-pluggable OSFP and QSFP-DD interfaces
- Low power dissipation of less than 0.1 W per end
- Commercial operating temperature range: 0°C to +70°C

Compliance

- Compliant with OSFP MSA
- Compliant with QSFP-DD MSA
- Compliant with CMIS 5.1
- Compliant with SFF-8679 electrical interface requirements
- Compliant with IEEE 802.3cd
- RoHS compliant

Applications

- 400G Ethernet
- AI/ML and High-Performance Computing (HPC)
- Data Center and Cloud Networking
- Switch-to-Server and Switch-to-NIC Interconnections
- Servers and Storage Systems

Description

The O400-QDD-C is a high-performance passive direct attach copper (DAC) cable designed for short-reach 400G interconnections in data center, cloud computing, and high-performance computing environments. It connects a 400G OSFP Flat Top port to a 400G QSFP-DD port and supports eight 53.125 Gb/s PAM4 electrical lanes, providing an aggregate raw electrical line rate of 425 Gb/s.

Featuring a passive shielded twinaxial copper architecture without active signal-conditioning components in the high-speed data path, the O400-QDD-C provides low-latency connectivity with low power consumption. Available in 26 AWG, 28 AWG and 30 AWG options and lengths from 1 m to 3 m, it is suitable for short-distance connections between switches, servers, network adapters, and storage systems.

The OSFP Flat Top interface is designed for OSFP-RHS host systems using a riding heatsink, while the QSFP-DD interface provides compatibility with high-density 400G QSFP-DD ports. The mixed-form-factor design enables direct 400G connectivity between OSFP- and QSFP-DD-based platforms without requiring optical transceivers or fiber patch cables.

The cable is designed in accordance with OSFP MSA, QSFP-DD MSA, CMIS 5.1, SFF-8679, IEEE 802.3cd, and RoHS requirements.

Product performance Specifications

1、Absolute Maximum Ratings

Parameter	Symbol	Min	Typ.	Max	Unit
Storage Temperature	TS	-40		+85	°C

2、Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit
Operating Case Temperature	TC	0		+70	°C
Power Supply Voltage	VCC	3.135	3.3	3.465	V
Relative Humidity	RH	5		85	%

3、General Product Specifications

Parameter	Specification	Condition
Product Type	Passive Direct Attach Copper (DAC) Cable	
Connector Configuration	400G OSFP Flat Top to 400G QSFP-DD	

Aggregate Data Rate	400 Gbps	
Raw Electrical Line Rate	425 Gbps	8 × 53.125 Gb/s
Electrical Signaling	PAM4	
Number of Channels	8 Full-Duplex Channels	
Data Rate per Lane	53.125 Gb/s	
Symbol Rate per Lane	26.5625 GBd	PAM4
Cable Length	1–3 m	
Cable Gauge	26 AWG, 28 AWG, 30 AWG	
Cable Type	Passive Shielded Twinaxial Copper	
Hot Pluggable	Supported	
Management Interface	I²C with EEPROM identification	

4、Power Supply and Electrical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit
Power Dissipation per End	PD			<0.1	W
Current per Signal Contact				0.5	A
Voltage per Contact				30	VDC
Low-Level Contact Resistance	LLCR			<2	Ω

5、High-Speed Signal Integrity Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Condition
Differential Impedance	Zdiff	90	100	110	Ω	TDR
Differential Insertion Loss	SDD21 / SDD12			17.16	dB	At 13.28 GHz

6、Frequency-Dependent Signal Integrity Limits

Parameter	Symbol	Frequency Range (GHz)	Requirement	Unit
Differential Return Loss	SDD11 / SDD22	0.05 ≤ f ≤ 4.1	SDD11/22(dB) < -16.5 + 2√f	dB
		4.1 < f ≤ 19	SDD11/22(dB) < -10.66 + 14log10(f/5.5)	dB
Common-Mode-to-Comm	SCC11 / SCC22	0.2 ≤ f ≤ 19	SCC11/22 ≤ -2	dB

on-Mode Return Loss				
Differential-to-Common-Mode Return Loss	SCD11 / SCD22	0.01 ≤ f ≤ 12.89	SCD11/22(dB) < -22 + (20/25.78)f	dB
		12.89 < f ≤ 19	SCD11/22(dB) < -15 + (6/25.78)f	dB
Differential-to-Common-Mode Conversion Loss	SCD21 − SDD21	0.01 ≤ f ≤ 12.89	SCD21 − SDD21 ≤ -10	dB
		12.89 < f ≤ 15.7	SCD21 − SDD21 ≤ -27 + (29/22)f	dB
		15.7 < f ≤ 19	SCD21 − SDD21 ≤ -6.3	dB

7、Cable Construction

Parameter	Specification
Cable Architecture	16 differential signal pairs (8 Tx + 8 Rx)
Cable Type	Shielded Twinaxial Copper
Conductor Material	Solid silver-plated copper
Conductor Gauge	26 AWG, 28 AWG, 30 AWG
Pair Drain Wire	28 AWG for 26 AWG cable; 30 AWG for 28 AWG and 30 AWG cable
Insulation Material	Foam polyolefin
Overall Cable Shield	Aluminum/polyester tape and tinned copper braid
Foil Coverage	125%
Braid Specification	38 AWG; 85% coverage

8、Cable Electrical and Physical Characteristics by AWG

Parameter	26 AWG	28 AWG	30 AWG	Unit
Differential Impedance	100±5	100±5	100±5	Ω
Mutual Capacitance	14	14	14	pF/ft
Propagation Delay	1.35	1.35	1.35	ns/ft
Intra-Pair Skew	120 ps / 8.5 m maximum	120 ps / 7 m maximum	50 ps / 5.5 m maximum	
Inter-Pair Skew	500 ps / 8.5 m maximum	500 ps / 7 m maximum	350 ps / 5.5 m maximum	
Conductor DC Resistance at 20°C (Typical)	0.041	0.065	0.103	Ω/ft

Outer Cable Diameter	5.2	4.7	4.2	mm

9、Mechanical Performance

Parameter	Test Condition	Specification	Unit
OSFP Mating Force	10 mm/min	≤40	N
QSFP-DD Mating Force	10 mm/min	≤90	N
OSFP Unmating Force	10 mm/min	≤30	N
QSFP-DD Unmating Force	10 mm/min	≤50	N
OSFP Latch Retention	Latch engaged	≥125	N
QSFP-DD Latch Retention	Latch engaged	≥90	N
Bulk Cable Retention in Module	Cable assembly only	≥90	N
Mechanical Durability	Plug/unplug cycles	≥50	Cycles
Minimum Bend Radius (Single Bend)		5 × Cable OD	
Minimum Bend Radius (Repeated Bending)		10 × Cable OD	

OSFP Pin-out Definition

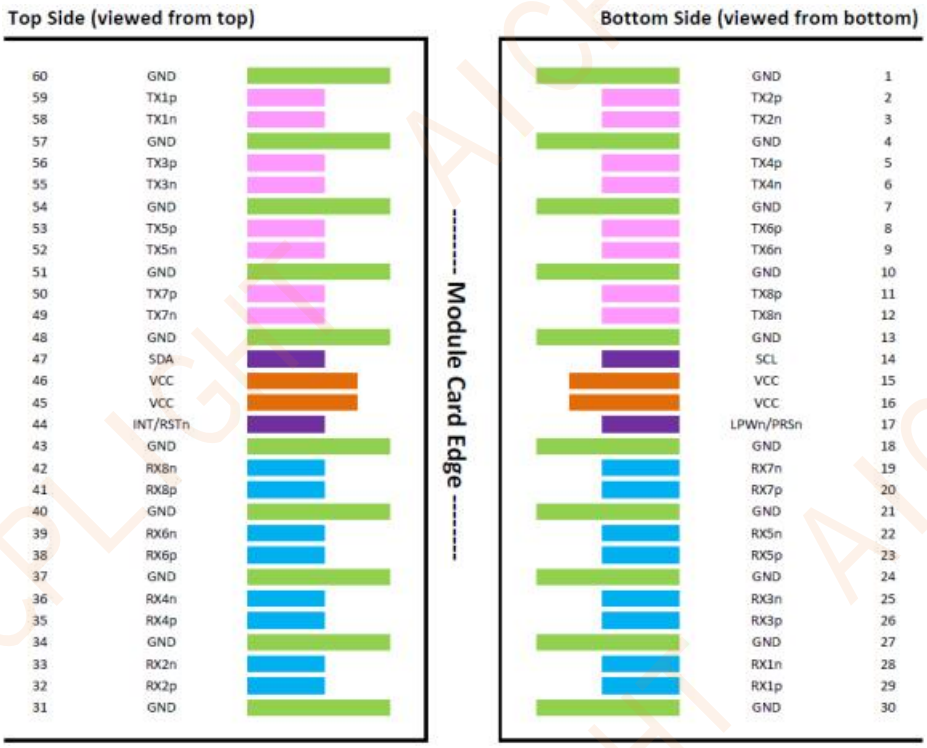

Figure4:Pin view(OSFP)

OSFP Pin Function Definitions

Pin	Logic	Symbol	Description	Note
1		GND	Ground	
2	CML-I	TX2p	Transmitter Data Non-Inverted	
3	CML-I	TX2n	Transmitter Data Inverted	
4		GND	Ground	
5	CML-I	TX4p	Transmitter Data Non-Inverted	
6	CML-I	TX4n	Transmitter Data Inverted	
7		GND	Ground	
8	CML-I	TX6p	Transmitter Data Non-Inverted	
9	CML-I	TX6n	Transmitter Data Inverted	
10		GND	Ground	
11	CML-I	TX8p	Transmitter Data Non-Inverted	
12	CML-I	TX8n	Transmitter Data Inverted	
13		GND	Ground	
14	LVCMOS-I/O	SCL	2-wire Serial interface clock	1
15		VCC	+3.3V Power	
16		VCC	+3.3V Power	
17	Multi-Level	LPWn/PRSn	Low-Power Mode / Module Present	2
18		GND	Ground	

19	CML-O	RX7n	Receiver Data Inverted	
20	CML-O	RX7p	Receiver Data Non-Inverted	
21		GND	Ground	
22	CML-O	RX5n	Receiver Data Inverted	
23	CML-O	RX5p	Receiver Data Non-Inverted	
24		GND	Ground	
25	CML-O	RX3n	Receiver Data Inverted	
26	CML-O	RX3p	Receiver Data Non-Inverted	
27		GND	Ground	
28	CML-O	RX1n	Receiver Data Inverted	
29	CML-O	RX1p	Receiver Data Non-Inverted	
30		GND	Ground	
31		GND	Ground	
32	CML-O	RX2p	Receiver Data Non-Inverted	
33	CML-O	RX2n	Receiver Data Inverted	
34		GND	Ground	
35	CML-O	RX4p	Receiver Data Non-Inverted	
36	CML-O	RX4n	Receiver Data Inverted	
37		GND	Ground	
38	CML-O	RX6p	Receiver Data Non-Inverted	
39	CML-O	RX6n	Receiver Data Inverted	
40		GND	Ground	
41	CML-O	RX8p	Receiver Data Non-Inverted	
42	CML-O	RX8n	Receiver Data Inverted	
43		GND	Ground	
44	Multi-Level	INT/RSTn	Module Interrupt / Module Reset	2
45		VCC	+3.3V Power	
46		VCC	+3.3V Power	
47	LVCMOS-I/O	SDA	2-wire Serial interface data	1
48		GND	Ground	
49	CML-I	TX7n	Transmitter Data Inverted	
50	CML-I	TX7p	Transmitter Data Non-Inverted	
51		GND	Ground	
52	CML-I	TX5n	Transmitter Data Inverted	
53	CML-I	TX5p	Transmitter Data Non-Inverted	
54		GND	Ground	
55	CML-I	TX3n	Transmitter Data Inverted	
56	CML-I	TX3p	Transmitter Data Non-Inverted	
57		GND	Ground	
58	CML-I	TX1n	Transmitter Data Inverted	

59	CML-I	TX1p	Transmitter Data Non-Inverted	
60		GND	Ground	

Note1: Open-Drain with pull up resistor on Host.

Note2: See pin description for required circut

QSFP-DD Pin-out Definition

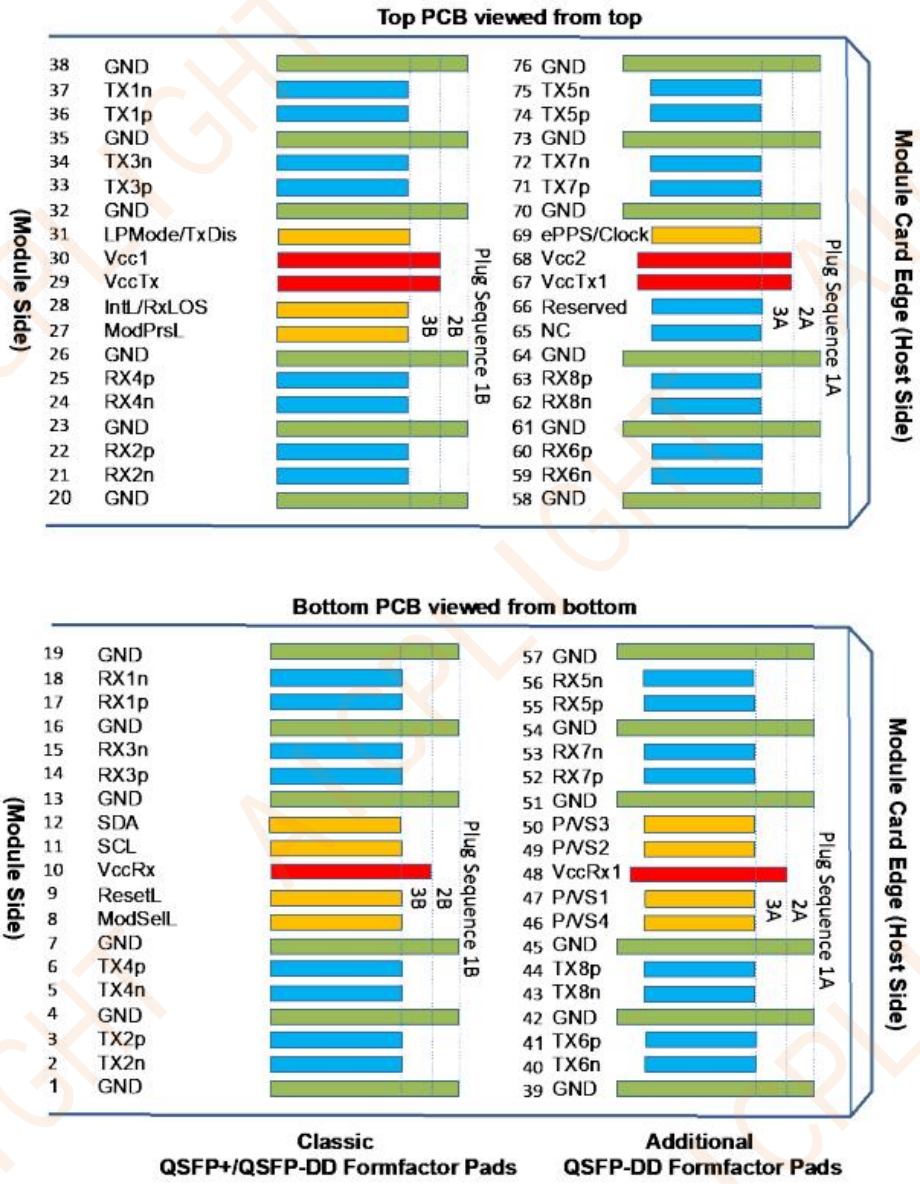

Figure4: Pin view

QSFP-DD Pin Function Definitions

Pin	Logic	Symbol	Description	Plug Sequence 4	Note
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		Vcc Rx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL/RxLOSL	Interrupt. Optionally configurable as RxLOSL via the management interface (SFF-8636)	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	

38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46	LVCMOS/CML-I	P/VS4	Programmable/Module Vendor Specific 4	3A	5
47	LVCMOS/CML-I	I P/VS1	Programmable/Module Vendor Specific 1	3A	5
48		VccRx1	3.3V Power Supply	2A	2
49	LVCMOS/CML-O	P/VS2	Programmable/Module Vendor Specific 2	3A	5
50	LVCMOS/CML-O	P/VS3	Programmable/Module Vendor Specific 3	3A	5
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	3A	
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	1A	1
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future Use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVCMOS-I	ePPS/Clock	1PPS PTP clock or reference clock input	3A	6
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Note1:QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFPDD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane. Each connector Gnd contact is rated for a steady state current of 500 mA.

Note2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Supply requirements defined for the host side of the Host Card Edge Connector are listed in Table 13. For power classes 4 and above the module differential loading of input

voltage pads must not result in exceeding contact current limits. Each connector Vcc contact is rated for a steady state current of 2000 mA.

Note3: Reserved pad recommended to be terminated with 10 kΩ to ground on the host. Pad 65 (No Connect) Shall be left unconnected within the module, optionally pad 65 may get terminated with 10 kΩ to ground on the host.

Note4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (See Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFPDD pads. Sequence 1A and 1B will then occur simultaneously, followed by 2A and 2B, followed by 3A and 3B.

Note5: Full definitions of the P/VSx signals currently under development. For module designs using programmable/vendor specific inputs P/VS1 and P/VS4 signals it is recommended each to be terminated in the module with 10 kΩ. For host designs using programmable/vendor specific outputs P/VS2 and P/VS3 signals it is recommended each to be terminated on the host with 10 kΩ.

Note6:for host not implementing ePPS/Clock, it is not necessary to parallel terminate the ePPS/Clock signal to ground on the host. ePPS/Clock already has parallel termination in the module see 4.2.6.

Monitoring Specification

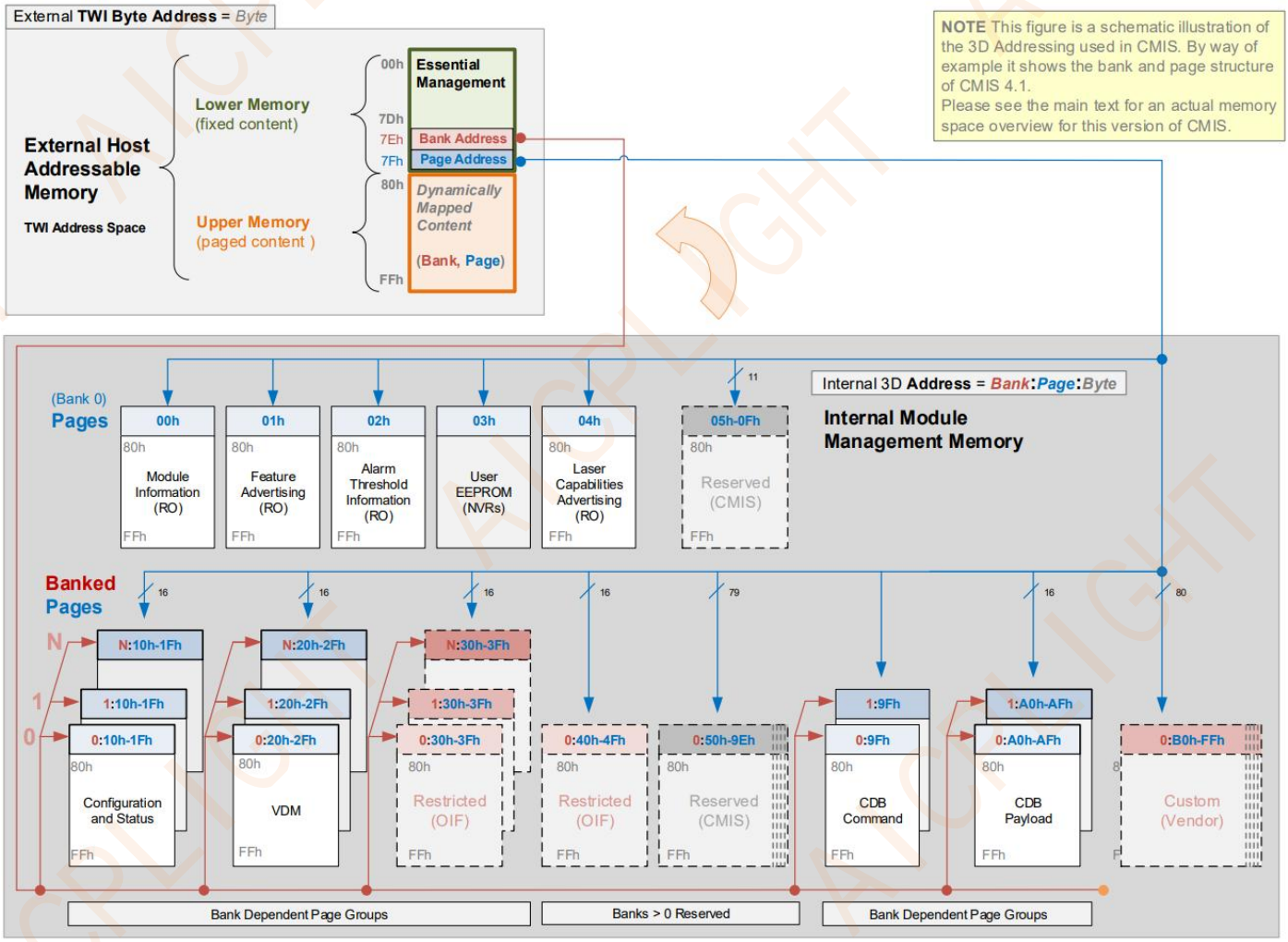

Figure5: Memory map

Memory map Table

Byte	Unit	Name	Description
		Lower Page 00h	
0-2	3	Management Characteristics	Basic Information about how this module is managed
3	1	Global Status Information	Current state of Module, Interrupt signal status
4-7	4	Flag Summary	Summary of Flags set on specific Pages (and Banks)
8-13	6	Module-Level Flags	Flags that are not lane or Data Path specific
14-25	12	Module-Level Monitors	Monitors that are not lane or Data Path specific
26-30	5	Module-Level Controls	Controls applicable to the module as a whole
31-36	6	Module-Level Masks	Mask bits for the Module-Level Flags
37-38	2	CDB Command Status	Status of current CDB command
39-40	2	Module Active Firmware Version	Module Active Firmware Version number
41	1	Fault Information	Fault cause for entering ModuleFault state
42-63	22		Reserved
64-84	21		Custom
85-117	33	Supported Applications Advertising	Applications supported by module Data Path(s)
118-125	8	Password Facilities	Password Entry and Change (mechanism only)
126-127	2	Page Mapping	Page mapping into host addressable Upper Memory
		Upper Page 00h	
128	1	SFF8024IdentifierCopy	Copy of Byte 00h:0
129-144	16	VendorName	Vendor name (ASCII)
145-147	3	Vendor OUI	Vendor IEEE company ID
148-163	16	Vendor PN	Part number provided by vendor (ASCII)
164-165	2	Vendor Rev	Revision level for part number provided by vendor (ASCII)
166-181	16	Vendor SN	Vendor Serial Number (ASCII)
182-189	8	DateCode	Manufacturing Date Code (ASCII)
190-199	10	CLEICode	Common Language Equipment Identification Code (ASCII)
200-201	2	ModulePowerCharacteristics	Module power characteristics
202	1	CableAssemblyLinkLength	Cable length (for cable assembly modules only)
203	1	ConnectorType	Connector type of the media interface
204-209	6	Copper Cable Attenuation	Attenuation characteristics (passive copper cables only)
210	1	MediaLaneInformation	Supported near end media lanes (all modules)
211	1	Cable Assembly Information	Far end modules information (cable assemblies only)
212	1	MediaInterfaceTechnology	Information on media side device or cable technology
213-220	8		Reserved
221	1		Custom
222	1	PageChecksum	Page Checksum over bytes 128-221
223-255	33		Custom

Mechanical Dimension



Note:

- All dimensions are in mm.
- Unless otherwise specified, dimensional tolerance is ±0.1 mm.
- Latch color: Black.
- Cable length tolerance: ±25 mm for L < 2 m and ±50 mm for L ≥ 2 m.

Handling and Safety Precautions:

- ESD Precautions: Follow standard ESD handling procedures when handling or installing the cable assembly, particularly at the connector ends.
- Bend Radius: Do not bend the cable below the specified minimum bend radius. Avoid sharp bends or repeated bending near the connector strain-relief area.
- Cable Handling: Avoid excessive pulling, twisting, crushing, kinking, or other mechanical stress that may damage the cable or affect signal integrity.
- Installation and Removal: Use the pull tab or release mechanism when inserting or removing the cable assembly. Do not pull directly on the cable.
- Connector Protection: Keep the electrical connector contacts clean and protected from dust, moisture, and contamination when not installed.
- Cable Assembly Protection: Do not disassemble, modify, splice, or attempt to repair the cable assembly or connector housing. Replace the cable if physical damage is observed.

Ordering Information

PN	Description
O400-QDD-C1	400G OSFP Flat Top to 400G QSFP-DD Passive Direct Attach Copper Twinax Cable,1m
O400-QDD-C1.5	400G OSFP Flat Top to 400G QSFP-DD Passive Direct Attach Copper Twinax Cable,1.5m
O400-QDD-C2	400G OSFP Flat Top to 400G QSFP-DD Passive Direct Attach Copper Twinax Cable,2m