Product Specification

800G OSFP Finned Top to 2× 400G QSFP112 InfiniBand NDR Passive Direct Attach Copper Breakout Cable

PN: O800-2Q-NDR-C



Features

- Supports InfiniBand NDR breakout connectivity
- Supports 800G to 2 × 400G breakout
- 8 × 106.25 Gb/s PAM4 electrical lanes
- 4 × 106.25 Gb/s PAM4 lanes per 400G branch
- 24–30 AWG cable options
- Available in 1–3 m lengths
- Passive twinax copper cable design
- Hot-pluggable OSFP and QSFP112 interfaces
- Low power dissipation of <0.1 W
- Commercial operating temperature range: 0°C to +70°C

Compliance

- InfiniBand Architecture Specification (IBTA), NDR
- OSFP MSA
- QSFP112 hardware and electrical interface requirements
- CMIS Rev. 5.1
- IEEE 802.3ck
- IEEE 802.3df-2024
- RoHS compliant

Applications

- InfiniBand NDR
- AI/ML clusters
- High-Performance Computing (HPC)
- GPU computing networks
- Cloud data centers
- NDR switch-to-NIC links

Description

The O800-2Q-NDR-C is a high-performance Passive Direct Attach Copper (DAC) breakout cable designed for InfiniBand NDR interconnections in AI, high-performance computing, and data center environments. It connects one 800G OSFP Finned Top interface to two independent 400G QSFP112 interfaces, supporting InfiniBand NDR breakout connectivity from one twin-port 800G interface to two 400 Gb/s NDR ports.

The 800G OSFP interface provides eight 106.25 Gb/s PAM4 electrical lanes, with four lanes allocated to each 400G QSFP112 branch. Featuring a passive twinaxial copper architecture without active signal-conditioning components in the high-speed data path, the cable provides low-latency and near-zero-power short-reach connectivity for compatible InfiniBand NDR switches, network adapters, DPUs, and systems.

Available in lengths from 1 m to 3 m and multiple conductor gauges from 24 AWG to 30 AWG, the cable is suitable for high-density interconnections in AI/ML clusters, HPC systems, and cloud data centers.

The OSFP Finned Top interface is designed for compatible twin-port switch interfaces, while each QSFP112 branch provides a four-lane 400G electrical interface for compatible host adapters and systems. The same 100G-PAM4 electrical architecture also supports compatible Ethernet applications.

The cable is designed in accordance with InfiniBand NDR requirements, OSFP MSA, applicable QSFP112 hardware and electrical interface requirements, CMIS Rev. 5.1, IEEE 802.3ck, IEEE 802.3df-2024, and RoHS requirements.

Product performance Specifications

1、Absolute Maximum Ratings

Parameter	Symbol	Min	Typ.	Max	Unit
Storage Temperature	TS	-40		+85	°C
Supply Voltage	VCC	-0.3		3.6	V
Relative Humidity	RH	5		85	%

2、Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit
Operating Case Temperature	TC	0		+70	°C
Power Supply Voltage	VCC	3.135	3.3	3.465	V
Relative Humidity	RH	5		85	%

3、General Product Specifications

Parameter	Specification	Condition
Product Type	Passive Direct Attach Copper (DAC) Breakout Cable	
Connector Configuration	1 × 800G OSFP Finned Top to 2 × 400G QSFP112	1-to-2 breakout
Supported Network Protocol	InfiniBand NDR / Ethernet	
InfiniBand Data Rate	NDR	
NDR Port Configuration	Twin-Port	2 × 400 Gb/s
Aggregate Data Rate	800 Gb/s	2 × 400 Gb/s
Raw Electrical Line Rate	850 Gb/s	8 × 106.25 Gb/s
Electrical Signaling	PAM4	
Data Rate per Lane	106.25 Gb/s	
Electrical Lane Configuration	8 Tx + 8 Rx at OSFP end; 4 Tx + 4 Rx per QSFP112 branch	
Host Electrical Interface	8-lane 100G-PAM4 to 2 × 4-lane 100G-PAM4	
Cable Length	1 m, 2 m, 3 m	
Cable Gauge	24–30 AWG	Depending on cable length and construction
Cable Type	Passive Twinaxial Copper	
Hot Pluggable	Supported	
Management Interface	I²C with EEPROM-based identification	

4、Breakout Lane Architecture

Parameter	Value
InfiniBand Interface	NDR
Breakout Architecture	1 × 800G to 2 × 400G
800G OSFP End	8 × 106.25 Gb/s PAM4 lanes
QSFP112 Branch 1	4 × 106.25 Gb/s PAM4 lanes
QSFP112 Branch 2	4 × 106.25 Gb/s PAM4 lanes
NDR Port Configuration	2 × 400 Gb/s
Modulation Format	PAM4
Signal Conditioning	Passive
Connector A	OSFP Finned Top
Connector B1 / B2	QSFP112

5、Power Supply and Management Interface

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Power Dissipation	PD			0.1	W	
I²C Clock Frequency	fSCL			400	kHz	
Contact Voltage Rating			30		VDC	Per contact; verify connector rating
Signal Contact Current Rating			0.5		A	Per contact; verify connector rating

6、High-Speed Signal Integrity Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Differential Insertion Loss	SDD21	11.0		19.75	dB	At 26.56 GHz
Reverse Differential Insertion Loss	SDD12	11.0		19.75	dB	At 26.56 GHz; subject to applicable compliance requirements
Minimum Cable Assembly Effective Return Loss	ERL	8.25			dB	Minimum cable assembly ERL
Channel Operating Margin	COM	3			dB	Minimum target under the applicable compliance test configuration

7、Frequency-Dependent Signal Integrity Limits

Parameter	Symbol	Frequency Range	Requirement	Unit
Differential-to-Common-Mode Return Loss	RLcd(f)	0.05 ≤ f < 26.56 GHz	RLcd(f) ≥ 22 − 10(f/26.56)	dB
		26.56 ≤ f ≤ 40 GHz	RLcd(f) ≥ 15 − 3(f/26.56)	dB
Differential-to-Common-Mode Conversion Loss Difference	SCD21 − SDD21	0.05 ≤ f < 12.89 GHz	SCD21 − SDD21 ≥ 10	dB
		12.89 ≤ f ≤ 40 GHz	SCD21 − SDD21 ≥ 14 − 0.3108f	dB
Common-Mode-to-Common-Mode Return Loss	RLcc(f)	0.05 ≤ f ≤ 6 GHz	RLcc(f) ≥ 1.4	dB
		6 < f ≤ 30 GHz	RLcc(f) ≥ 0.68 + 0.12f	dB
		30 < f ≤ 40 GHz	RLcc(f) ≥ 10.28 − 0.2f	dB

8、Cable Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Differential Impedance	Zdiff	95	100	105	Ω	TDR measurement
Mutual Capacitance	Cm		14		pF/ft	Nominal reference
Propagation Delay	tp		1.31–1.35		ns/ft	Depending on cable gauge
Propagation Delay	tp		4.30–4.43		ns/m	Approximate equivalent

9、Cable Electrical and Physical Characteristics by AWG

Parameter	24 AWG	26 AWG	28 AWG	30 AWG	Unit
Intra-Pair Skew	80 ps / 10 m max.	120 ps / 8.5 m max.	120 ps / 7 m max.	50 ps / 5.5 m max.	ps / reference length
Inter-Pair Skew	350 ps / 10 m max.	500 ps / 8.5 m max.	500 ps / 7 m max.	350 ps / 5.5 m max.	ps / reference length
Conductor DC Resistance at 20°C	0.026	0.041	0.065	0.103	Ω/ft, reference values
Outer Cable Diameter	6.0	5.2	4.7	4.2	mm

10、Cable Construction

Parameter	Value
Cable Architecture	16 differential pairs total (8 Tx + 8 Rx), with 4 Tx + 4 Rx differential pairs assigned to each QSFP112 branch
Conductor Material	Solid silver-plated copper, subject to actual cable construction
Pair Drain Wire	26 AWG for 24 AWG cable; 28 AWG for 26 AWG cable; 30 AWG for 28/30 AWG cable
Insulation Material	Foam polyolefin
Overall Cable Shield	Aluminum/polyester foil and tinned copper braid
Braid Specification	38 AWG; 85% coverage
Foil Coverage	125%, according to the original cable construction data
Cable Jacket	PVC or LSZH, depending on the selected construction

11、Mechanical Performance

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
OSFP Mating Force				40	N	Per connector specification
QSFP112 Mating Force				60	N	Per connector specification
OSFP Unmating Force				30	N	Per connector specification
QSFP112 Unmating Force				30	N	Per connector specification
Latch Retention Force		125			N	Minimum; test configuration dependent
Bulk Cable Retention in Module		90			N	Minimum; test configuration dependent
Mechanical Durability		50			Cycles	Minimum mating/unmating cycles
Minimum Bend Radius, Single Bend				5 × cable OD		Subject to cable construction
Minimum Bend Radius, Repeated Bending				10 × cable OD		

Pin-out Definition(OSFP)

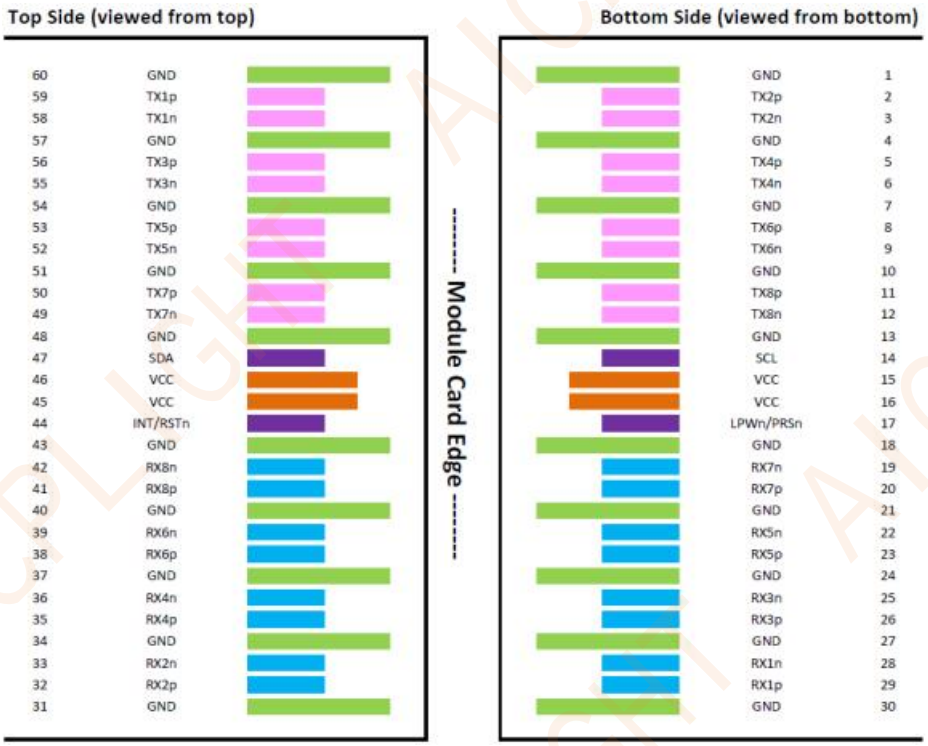


Figure4: Pin view(OSFP)

Pin Function Definitions(OSFP)

Pin	Logic	Symbol	Description	Note
1		GND	Ground	
2	CML-I	TX2p	Transmitter Data Non-Inverted	
3	CML-I	TX2n	Transmitter Data Inverted	
4		GND	Ground	
5	CML-I	TX4p	Transmitter Data Non-Inverted	
6	CML-I	TX4n	Transmitter Data Inverted	
7		GND	Ground	
8	CML-I	TX6p	Transmitter Data Non-Inverted	
9	CML-I	TX6n	Transmitter Data Inverted	
10		GND	Ground	
11	CML-I	TX8p	Transmitter Data Non-Inverted	
12	CML-I	TX8n	Transmitter Data Inverted	
13		GND	Ground	
14	LVCMOS-I/O	SCL	2-wire Serial interface clock	1
15		VCC	+3.3V Power	
16		VCC	+3.3V Power	

17	Multi-Level	LPWn/PRSn	Low-Power Mode / Module Present	2
18		GND	Ground	
19	CML-O	RX7n	Receiver Data Inverted	
20	CML-O	RX7p	Receiver Data Non-Inverted	
21		GND	Ground	
22	CML-O	RX5n	Receiver Data Inverted	
23	CML-O	RX5p	Receiver Data Non-Inverted	
24		GND	Ground	
25	CML-O	RX3n	Receiver Data Inverted	
26	CML-O	RX3p	Receiver Data Non-Inverted	
27		GND	Ground	
28	CML-O	RX1n	Receiver Data Inverted	
29	CML-O	RX1p	Receiver Data Non-Inverted	
30		GND	Ground	
31		GND	Ground	
32	CML-O	RX2p	Receiver Data Non-Inverted	
33	CML-O	RX2n	Receiver Data Inverted	
34		GND	Ground	
35	CML-O	RX4p	Receiver Data Non-Inverted	
36	CML-O	RX4n	Receiver Data Inverted	
37		GND	Ground	
38	CML-O	RX6p	Receiver Data Non-Inverted	
39	CML-O	RX6n	Receiver Data Inverted	
40		GND	Ground	
41	CML-O	RX8p	Receiver Data Non-Inverted	
42	CML-O	RX8n	Receiver Data Inverted	
43		GND	Ground	
44	Multi-Level	INT/RSTn	Module Interrupt / Module Reset	2
45		VCC	+3.3V Power	
46		VCC	+3.3V Power	
47	LVCMOS-I/O	SDA	2-wire Serial interface data	1
48		GND	Ground	
49	CML-I	TX7n	Transmitter Data Inverted	
50	CML-I	TX7p	Transmitter Data Non-Inverted	
51		GND	Ground	
52	CML-I	TX5n	Transmitter Data Inverted	
53	CML-I	TX5p	Transmitter Data Non-Inverted	
54		GND	Ground	
55	CML-I	TX3n	Transmitter Data Inverted	
56	CML-I	TX3p	Transmitter Data Non-Inverted	

57		GND	Ground	
58	CML-I	TX1n	Transmitter Data Inverted	
59	CML-I	TX1p	Transmitter Data Non-Inverted	
60		GND	Ground	

Note1: Open-Drain with pull up resistor on Host.

Note2: See pin description for required circuit.

Pin-out Definition(QSFP112)

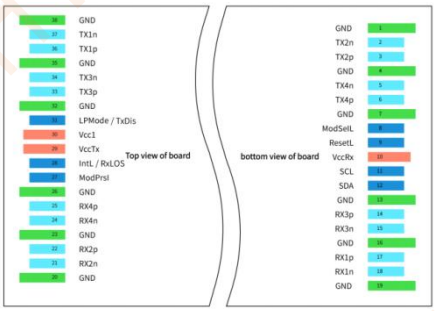


Figure4:QSFP112 Module contact assignment



Figure5: Pin view

Pin Function Definitions(QSFP112)

PIN	Module contact	Logic	Symbol	Description	Note
1	1		GND	Ground	1
2			GND	Ground	1
3	2	CML-I	Tx2n	Transmitter Inverted Data Input	
4	3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
5	4		GND	Ground	1
6			GND	Ground	1
7	5	CML-I	Tx4n	Transmitter Inverted Data Input	
8	6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
9	7		GND	Ground	1
10			GND	Ground	1
11	8	LVTTL-I	ModSelL	Select	
12	9	LVTTL-1	ResetL	Reset	
13	10		Vcc Rx	+3.3V Power supply receiver	2
14			Vcc Rx	+3.3V Power supply receiver	2
15	11	LVCMOS-I/O	SCL	2-wire serial interface clock	
16	12	LVCMOS-I/O	SDA	2-wire serial interface data	
17	13		GND	Ground	1
18			GND	Ground	1
19	14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
20	15	CML-O	Rx3n	Receiver Inverted Data Output	
21	16		GND	Ground	1
22			GND	Ground	1
23	17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
24	18	CML-O	Rx1n	Receiver Inverted Data Output	
25	19		GND	Ground	1
26			GND	Ground	1
27	20		GND	Ground	1
28			GND	Ground	1
29	21	CML-O	Rx2n	Receiver Inverted Data Output	
30	22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
31	23		GND	Ground	1
32			GND	Ground	1
33	24	CML-O	Rx4n	Receiver Inverted Data Output	
34	25	CML-O	Rx4p	Receiver Non-Inverted Data Output	

35	26		GND	Ground	1
36			GND	Ground	1
37	27	LVTTL-O	ModPrsL	Present	
38	28	LVTTL-O	IntL/RxLOS	Interrupt/optional RxLOS	
39	29		Vcc Tx	+3.3V Power supply transmitter	2
40			Vcc Tx	+3.3V Power supply transmitter	2
41	30		$Vcc1_2$	+3.3V Power Supply	2
42	31	LVTTL-I	LPMode/TxD is	Low Power Mode/optional TX Disable	
43	32		GND	Ground	1
44			GND	Ground	1
45	33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
46	34	CML-I	Tx3n	Transmitter Inverted Data Input	
47	35		GND	Ground	1
48			GND	Ground	1
49	36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
50	37	CML-I	Tx1n	Transmitter Inverted Data Input	
51	38		GND	Ground	1
52			GND	Ground	1

Note1:GND is the symbol for signal and supply(power)common for the QSFP112module.Allare common within the QSFP112 module and all voltages are referenced to this potential unless otherwise noted.Connect these directly to the host board signal-common ground plane.

Note2: Vcc Rx,Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements,defined for the host side of the Host Edge Card Connector,are listed in Table 4.Recommended host board power supply fitering is shown in Figure 4.Vcc Rx,Vecc1and Vcc Tx may be intemally connected within the QSFP112 module in any combination.The connector pins are each rated for amaximum current of 1.5A(max.current of 2.0 Ais required for high module power of15-20W).

Monitoring Specification

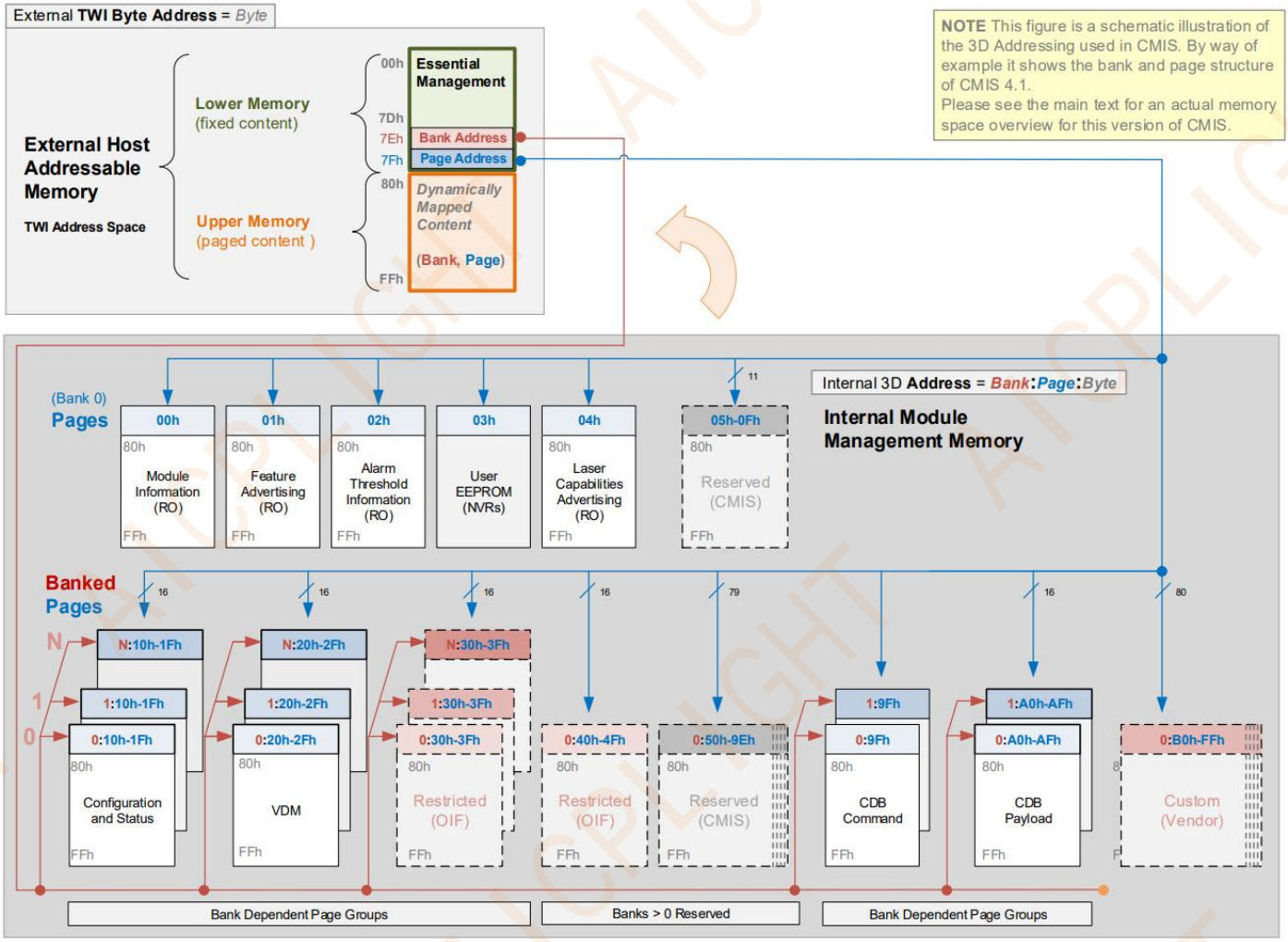


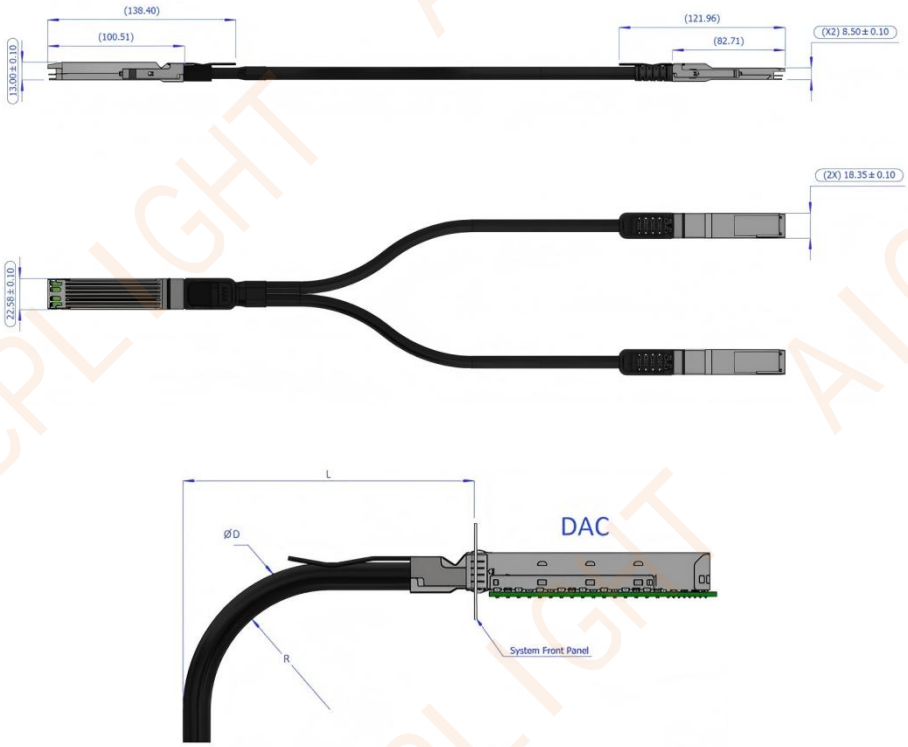
Figure5: Memory map

Memory map Table

Byte	Unit	Name	Description
Lower Page 00h			
0-2	3	Management Characteristics	Basic Information about how this module is managed
3	1	Global Status Information	Current state of Module, Interrupt signal status
4-7	4	Flag Summary	Summary of Flags set on specific Pages (and Banks)
8-13	6	Module-Level Flags	Flags that are not lane or Data Path specific
14-25	12	Module-Level Monitors	Monitors that are not lane or Data Path specific
26-30	5	Module-Level Controls	Controls applicable to the module as a whole
31-36	6	Module-Level Masks	Mask bits for the Module-Level Flags
37-38	2	CDB Command Status	Status of current CDB command

39-40	2	Module Active Firmware Version	Module Active Firmware Version number
41	1	Fault Information	Fault cause for entering ModuleFault state
42-63	22		Reserved
64-84	21		Custom
85-117	33	Supported Applications Advertising	Applications supported by module Data Path(s)
118-125	8	Password Facilities	Password Entry and Change (mechanism only)
126-127	2	Page Mapping	Page mapping into host addressable Upper Memory
Upper Page 00h			
128	1	SFF8024IdentifierCopy	Copy of Byte 00h:0
129-144	16	VendorName	Vendor name (ASCII)
145-147	3	Vendor OUI	Vendor IEEE company ID
148-163	16	Vendor PN	Part number provided by vendor (ASCII)
164-165	2	Vendor Rev	Revision level for part number provided by vendor (ASCII)
166-181	16	Vendor SN	Vendor Serial Number (ASCII)
182-189	8	DateCode	Manufacturing Date Code (ASCII)
190-199	10	CLEICode	Common Language Equipment Identification Code (ASCII)
200-201	2	ModulePowerCharacteristics	Module power characteristics
202	1	CableAssemblyLinkLength	Cable length (for cable assembly modules only)
203	1	ConnectorType	Connector type of the media interface
204-209	6	Copper Cable Attenuation	Attenuation characteristics (passive copper cables only)
210	1	MediaLaneInformation	Supported near end media lanes (all modules)
211	1	Cable Assembly Information	Far end modules information (cable assemblies only)
212	1	MediaInterfaceTechnology	Information on media side device or cable technology
213-220	8		Reserved
221	1		Custom
222	1	PageChecksum	Page Checksum over bytes 128-221
223-255	33		Custom

Mechanical Dimension



Note:

- All dimensions are in mm.
- Unless otherwise specified, dimensional tolerance is ±0.1 mm.
- Latch color: Black.
- Cable length tolerance: ±25 mm for L < 2 m and ±50 mm for L ≥ 2 m.

Handling and Safety Precautions:

- ESD Precautions: Follow standard ESD handling procedures when handling or installing the cable assembly, particularly at the connector ends.
- Bend Radius: Do not bend the cable below the specified minimum bend radius. Avoid sharp bends or repeated bending near the connector strain-relief area.
- Cable Handling: Avoid excessive pulling, twisting, crushing, kinking, or other mechanical stress that may damage the cable or affect signal integrity.
- Installation and Removal: Use the pull tab or release mechanism when inserting or removing the cable assembly. Do not pull directly on the cable.
- Connector Protection: Keep the electrical connector contacts clean and protected from dust, moisture, and contamination when not installed.
- Cable Assembly Protection: Do not disassemble, modify, splice, or attempt to repair the cable assembly or connector housing. Replace the cable if physical damage is observed.

Ordering Information

PN	Description
O800-2Q-NDR-C1	800G OSFP Finned Top to 2× 400G QSFP112 InfiniBand NDR Passive Direct Attach Copper Breakout Cable,1m
O800-2Q-NDR-C1.5	800G OSFP Finned Top to 2× 400G QSFP112 InfiniBand NDR Passive Direct Attach Copper Breakout Cable,1.5m
O800-2Q-NDR-C2	800G OSFP Finned Top to 2× 400G QSFP112 InfiniBand NDR Passive Direct Attach Copper Breakout Cable,2m
O800-2Q-NDR-C3	800G OSFP Finned Top to 2× 400G QSFP112 InfiniBand NDR Passive Direct Attach Copper Breakout Cable,3m