Product Specification

3~5m 800G OSFP Finned Top to 4× 200G QSFP112 Active Copper Breakout Cable

PN: O800-4Q200-AC



Features

- Supports 800G to 4×200G breakout connectivity
- 8 × 106.25 Gb/s PAM4 electrical lanes
- Two electrical lanes allocated to each 200G QSFP112 branch
- 53.125 GBd symbol rate per electrical lane
- Active signal-conditioning architecture
- Wire gauge: 26 AWG and 30 AWG
- Available in 3–5 m lengths
- Hot-pluggable OSFP and QSFP112 interfaces
- OSFP Finned Top host connector for integrated thermal management
- Single 3.3 V power supply
- Two-wire management interface with EEPROM identification
- Commercial operating temperature range: 0°C to +70°C

Compliance

- Compliant with OSFP MSA Rev. 5.22
- Compliant with SFF-8665 QSFP112 pluggable interface requirements
- Compliant with SFF-TA-1027 QSFP112 mechanical interface requirements
- Compliant with SFF-8679 QSFP hardware and electrical interface requirements
- Designed for OSFP 800GAUI-8 electrical interface architecture
- Designed in accordance with applicable IEEE 802.3ck 100G-per-lane electrical requirements
- CMIS-compliant management interface
- RoHS compliant

Applications

- 800G to 4×200G Breakout Connectivity
- AI/ML and GPU Computing Networks
- High-Performance Computing (HPC)
- Hyperscale Data Centers and Cloud Networking
- Switch-to-Server and Switch-to-NIC Interconnections
- High-Density Rack-Level Network InterconnectionsData center cabling infrastructure
- High density connections between networking equipment

Description

The O800-4Q200-AC is a high-performance Active Copper Cable (ACC) breakout assembly designed for short-reach, high-bandwidth interconnections in AI computing, high-performance computing, and hyperscale data center environments. It connects one 800G OSFP Finned Top interface to four independent 200G QSFP112 interfaces, enabling 800G-to-4 × 200G breakout connectivity.

The 800G host end utilizes eight 106.25 Gb/s PAM4 electrical lanes, with two lanes allocated to each 200G QSFP112 branch. Each electrical lane operates at 53.125 GBd PAM4, resulting in a raw electrical line rate of 850 Gb/s at the OSFP host end and 212.5 Gb/s for each 200G branch.

Integrated active signal-conditioning electronics compensate for high-frequency copper-channel loss and extend the usable copper reach beyond conventional passive DAC solutions while maintaining low latency. The OSFP Finned Top host connector incorporates an integrated heatsink for thermal management in high-density switching environments, while the four QSFP112 branch connectors provide compact 200G connectivity for servers, network adapters, and accelerator systems.

The cable is available in 30 AWG and 26 AWG configurations with lengths of 3~5m. A two-wire management interface provides EEPROM-based product identification, configuration information, and cable management functions.

The O800-4Q200-AC is designed in accordance with OSFP MSA, applicable QSFP112 interface specifications, IEEE 802.3ck electrical requirements, CMIS management requirements, and RoHS regulations.

Product Performance Specifications

1、Absolute Maximum Ratings

Parameter	Symbol	Min	Typ.	Max	Unit
Storage Temperature	TS	-40		+85	°C
Supply Voltage	VCC	-0.3		+3.6	V

2、Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit
Operating Case Temperature	TC	0		+70	°C
Power Supply Voltage	VCC	3.135	3.3	3.465	V
Relative Humidity	RH	5		85	%

3、General Product Specifications

Parameter	Specification	Condition
Product Type	Active Copper Cable (ACC) Breakout Cable	
Connector Configuration	1 × 800G OSFP Finned Top to 4 × 200G QSFP112	1-to-4 breakout
Aggregate Data Rate	800 Gbps	4 × 200 Gbps
Raw Electrical Line Rate	850 Gbps	8 × 106.25 Gb/s
Raw Electrical Line Rate per Branch	212.5 Gbps	2 × 106.25 Gb/s
Electrical Signaling	PAM4	
Number of Host Data Lanes	8 Full-Duplex Lanes	
Number of Data Lanes per Branch	2 Full-Duplex Lanes	
Data Rate per Lane	106.25 Gb/s	
Symbol Rate per Lane	53.125 GBd	PAM4
Electrical Lane Configuration	8 Tx + 8 Rx differential pairs at the OSFP end; 2 Tx + 2 Rx differential pairs per QSFP112 branch	
Host Electrical Interface	800GAUI-8	
Branch Electrical Interface	200GAUI-2	
Cable Length	3 m,4m, 5 m	
Cable Gauge	26 AWG, 30 AWG	
Cable Type	Active Shielded Twinaxial Copper	
Host Connector Thermal Design	Finned Top	
Hot Pluggable	Supported	
Active Signal Conditioning	Supported	
Management Interface	Two-wire serial interface	
Module Identification	EEPROM	

4、Power Supply and Management Interface

Parameter	Symbol	Min	Typ.	Max	Unit
Power Supply Voltage	VCC	3.135	3.3	3.465	V
Management Interface			Two-wire serial interface		
Module Identification			EEPROM		
Management Architecture			CMIS		

5、High-Speed Electrical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Condition
Differential Impedance	Zdiff	90	100	110	Ω	Differential
Symbol Rate per Lane	SRL		53.125		GBd	PAM4
Raw Electrical Line Rate per Lane	DRL		106.25		Gb/s	PAM4
Effective Data Rate per Lane			100		Gb/s	
Host Electrical Lanes			8			Per direction
Electrical Lanes per Branch			2			Per direction
Aggregate Data Rate			800		Gb/s	
Data Rate per Branch			200		Gb/s	
Active Signal Conditioning			Supported			

6、Active Signal Conditioning and Lane Architecture

Parameter	Specification
Host Electrical Interface	800GAUI-8
Branch Electrical Interface	200GAUI-2
Signaling Architecture	8 × 100G-class PAM4
PAM4 Symbol Rate	53.125 GBd
Host Transmit Lanes	8 differential lanes
Host Receive Lanes	8 differential lanes
Branch Transmit Lanes	2 differential lanes per branch
Branch Receive Lanes	2 differential lanes per branch
Total Differential Signal Pairs	16
Raw Electrical Rate per Lane	106.25 Gb/s
Host Raw Electrical Line Rate	850 Gb/s
Raw Electrical Line Rate per Branch	212.5 Gb/s
Active Equalization	Supported
Signal Loss Compensation	Supported
Lane Mapping	8 lanes to 4 × 2 lanes

7、Cable Construction

Parameter	Specification

Cable Architecture	16 differential signal pairs total (8 Tx + 8 Rx)
Breakout Architecture	4 × 4-pair branch cable groups
Cable Type	Shielded Active Twinaxial Copper
Conductor Gauge	26 AWG, 30 AWG
Differential Impedance	100 Ω nominal
High-Speed Signaling	106.25 Gb/s PAM4 per lane
Signal Conditioning	Integrated active equalization electronics
Cable Management	EEPROM-based identification and configuration
Host Connector	OSFP Finned Top
Branch Connectors	4 × QSFP112

8、Cable Configuration by Length

Cable Length	Wire Gauge	Host Connector	Branch Connectors
3 m	30 AWG	OSFP Finned Top	4 × QSFP112
4 m	30 AWG	OSFP Finned Top	4 × QSFP112
5 m	26 AWG	OSFP Finned Top	4 × QSFP112

9、Mechanical Interface

Parameter	Specification
Host Connector Form Factor	OSFP
Host Connector Top Type	Finned Top
Branch Connector Form Factor	QSFP112
Number of Branch Connectors	4
Host High-Speed Lanes	8 per direction
Branch High-Speed Lanes	2 per direction per branch
Total Differential Signal Pairs	16
Latching Mechanism	Pull-to-release

10、Environmental and Regulatory Characteristics

Parameter	Specification

Operating Temperature	0°C to +70°C
Storage Temperature	-40°C to +85°C
Operating Relative Humidity	5% to 85%
RoHS	Compliant

Pin-out Definition(OSFP)

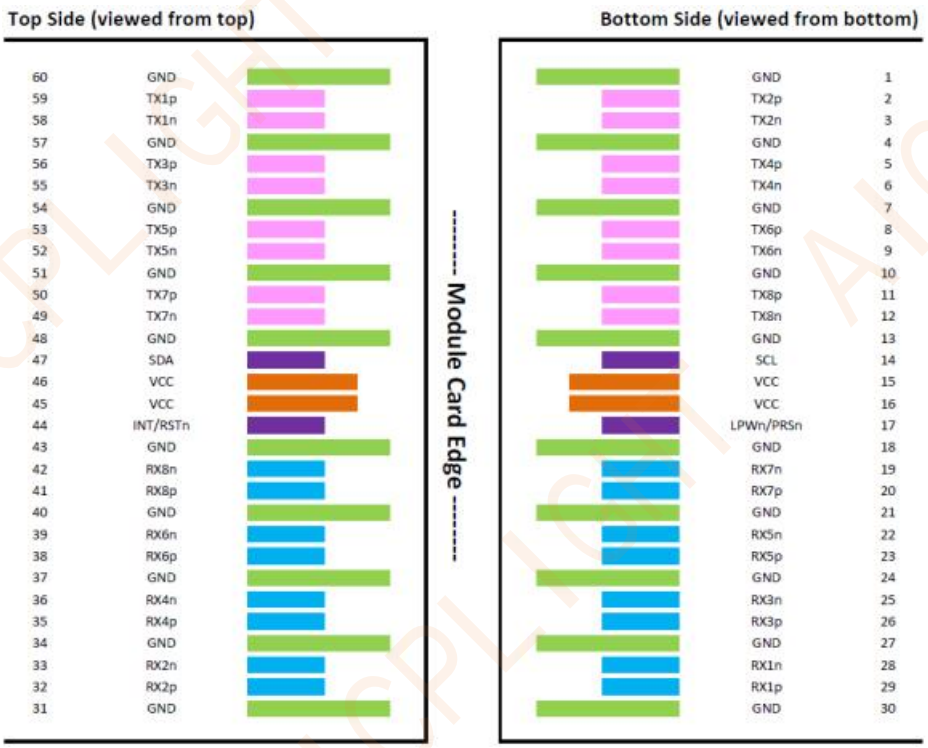


Figure4: Pin view(OSFP)

Pin Function Definitions(OSFP)

Pin	Logic	Symbol	Description	Note
1		GND	Ground	
2	CML-I	TX2p	Transmitter Data Non-Inverted	
3	CML-I	TX2n	Transmitter Data Inverted	
4		GND	Ground	
5	CML-I	TX4p	Transmitter Data Non-Inverted	
6	CML-I	TX4n	Transmitter Data Inverted	
7		GND	Ground	
8	CML-I	TX6p	Transmitter Data Non-Inverted	
9	CML-I	TX6n	Transmitter Data Inverted	
10		GND	Ground	

11	CML-I	TX8p	Transmitter Data Non-Inverted	
12	CML-I	TX8n	Transmitter Data Inverted	
13		GND	Ground	
14	LVCMOS-I/O	SCL	2-wire Serial interface clock	1
15		VCC	+3.3V Power	
16		VCC	+3.3V Power	
17	Multi-Level	LPWn/PRSn	Low-Power Mode / Module Present	2
18		GND	Ground	
19	CML-O	RX7n	Receiver Data Inverted	
20	CML-O	RX7p	Receiver Data Non-Inverted	
21		GND	Ground	
22	CML-O	RX5n	Receiver Data Inverted	
23	CML-O	RX5p	Receiver Data Non-Inverted	
24		GND	Ground	
25	CML-O	RX3n	Receiver Data Inverted	
26	CML-O	RX3p	Receiver Data Non-Inverted	
27		GND	Ground	
28	CML-O	RX1n	Receiver Data Inverted	
29	CML-O	RX1p	Receiver Data Non-Inverted	
30		GND	Ground	
31		GND	Ground	
32	CML-O	RX2p	Receiver Data Non-Inverted	
33	CML-O	RX2n	Receiver Data Inverted	
34		GND	Ground	
35	CML-O	RX4p	Receiver Data Non-Inverted	
36	CML-O	RX4n	Receiver Data Inverted	
37		GND	Ground	
38	CML-O	RX6p	Receiver Data Non-Inverted	
39	CML-O	RX6n	Receiver Data Inverted	
40		GND	Ground	
41	CML-O	RX8p	Receiver Data Non-Inverted	
42	CML-O	RX8n	Receiver Data Inverted	
43		GND	Ground	
44	Multi-Level	INT/RSTn	Module Interrupt / Module Reset	2
45		VCC	+3.3V Power	
46		VCC	+3.3V Power	
47	LVCMOS-I/O	SDA	2-wire Serial interface data	1
48		GND	Ground	
49	CML-I	TX7n	Transmitter Data Inverted	
50	CML-I	TX7p	Transmitter Data Non-Inverted	

51		GND	Ground	
52	CML-I	TX5n	Transmitter Data Inverted	
53	CML-I	TX5p	Transmitter Data Non-Inverted	
54		GND	Ground	
55	CML-I	TX3n	Transmitter Data Inverted	
56	CML-I	TX3p	Transmitter Data Non-Inverted	
57		GND	Ground	
58	CML-I	TX1n	Transmitter Data Inverted	
59	CML-I	TX1p	Transmitter Data Non-Inverted	
60		GND	Ground	

Note1: Open-Drain with pull up resistor on Host.

Note2: See pin description for required circuit.

Pin-out Definition(QSFP112)

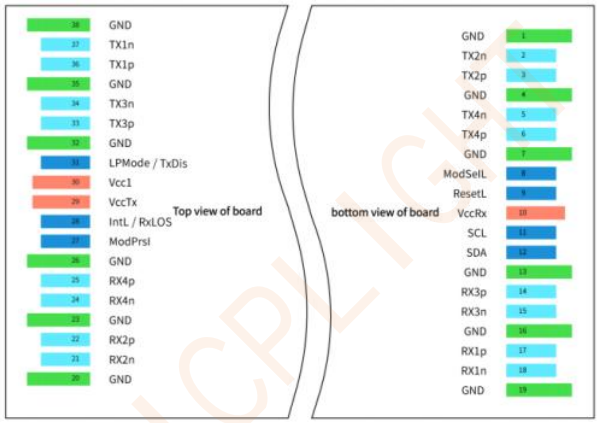


Figure4:QSFP112 Module contact assignment



Figure5: Pin view

Pin Function Definitions(QSFP112)

PIN	Module contact	Logic	Symbol	Description	Note
1	1		GND	Ground	1
2			GND	Ground	1
3	2	CML-I	Tx2n	Transmitter Inverted Data Input	
4	3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
5	4		GND	Ground	1
6			GND	Ground	1
7	5	CML-I	Tx4n	Transmitter Inverted Data Input	
8	6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
9	7		GND	Ground	1
10			GND	Ground	1
11	8	LVTTL-I	ModSelL	Select	
12	9	LVTTL-1	ResetL	Reset	
13	10		Vcc Rx	+3.3V Power supply receiver	2
14			Vcc Rx	+3.3V Power supply receiver	2
15	11	LVCMOS-I/O	SCL	2-wire serial interface clock	
16	12	LVCMOS-I/O	SDA	2-wire serial interface data	
17	13		GND	Ground	1
18			GND	Ground	1
19	14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
20	15	CML-O	Rx3n	Receiver Inverted Data Output	
21	16		GND	Ground	1
22			GND	Ground	1
23	17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
24	18	CML-O	Rx1n	Receiver Inverted Data Output	
25	19		GND	Ground	1
26			GND	Ground	1
27	20		GND	Ground	1
28			GND	Ground	1
29	21	CML-O	Rx2n	Receiver Inverted Data Output	
30	22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
31	23		GND	Ground	1
32			GND	Ground	1
33	24	CML-O	Rx4n	Receiver Inverted Data Output	
34	25	CML-O	Rx4p	Receiver Non-Inverted Data Output	

35	26		GND	Ground	1
36			GND	Ground	1
37	27	LVTTL-O	ModPrsL	Present	
38	28	LVTTL-O	IntL/RxLOS	Interrupt/optional RxLOS	
39	29		Vcc Tx	+3.3V Power supply transmitter	2
40			Vcc Tx	+3.3V Power supply transmitter	2
41	30		$Vcc1_2$	+3.3V Power Supply	2
42	31	LVTTL-I	LPMode/TxD is	Low Power Mode/optional TX Disable	
43	32		GND	Ground	1
44			GND	Ground	1
45	33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
46	34	CML-I	Tx3n	Transmitter Inverted Data Input	
47	35		GND	Ground	1
48			GND	Ground	1
49	36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
50	37	CML-I	Tx1n	Transmitter Inverted Data Input	
51	38		GND	Ground	1
52			GND	Ground	1

Note1:GND is the symbol for signal and supply(power)common for the QSFP112module.Allare common within the QSFP112 module and all voltages are referenced to this potential unless otherwise noted.Connect these directly to the host board signal-common ground plane.

Note2: Vcc Rx,Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements,defined for the host side of the Host Edge Card Connector,are listed in Table 4.Recommended host board power supply fitering is shown in Figure 4.Vcc Rx,Vecc1and Vcc Tx may be intemally connected within the QSFP112 module in any combination.The connector pins are each rated for amaximum current of 1.5A(max.current of 2.0 Ais required for high module power of15-20W).

Monitoring Specification

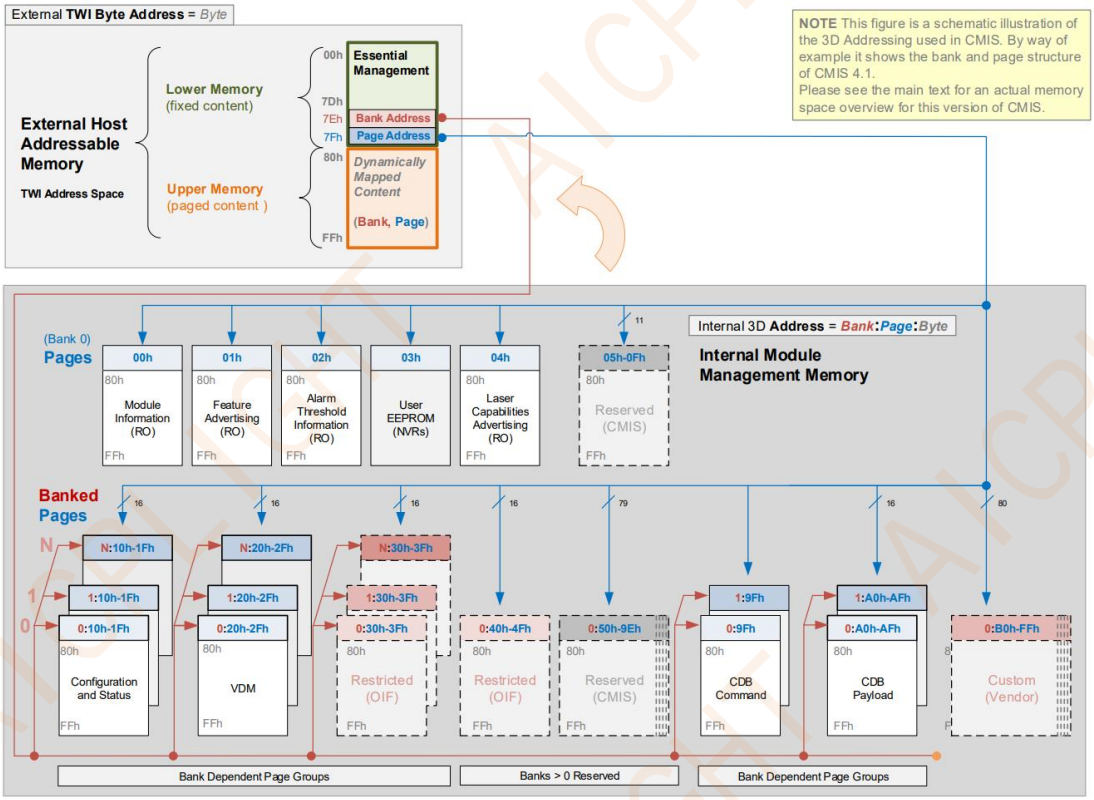


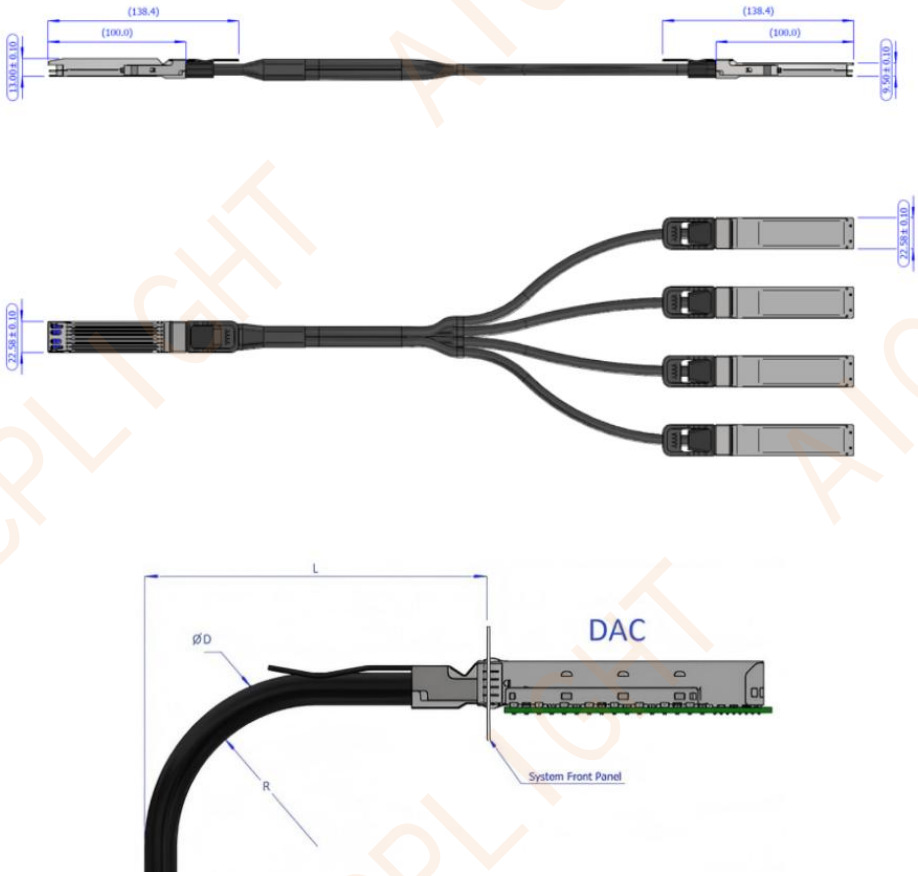
Figure5:Memory map

Memory map Table

Byte	Unit	Name	Description
		Lower Page 00h	
0-2	3	Management Characteristics	Basic Information about how this module is managed
3	1	Global Status Information	Current state of Module, Interrupt signal status
4-7	4	Flag Summary	Summary of Flags set on specific Pages (and Banks)
8-13	6	Module-Level Flags	Flags that are not lane or Data Path specific
14-25	12	Module-Level Monitors	Monitors that are not lane or Data Path specific
26-30	5	Module-Level Controls	Controls applicable to the module as a whole
31-36	6	Module-Level Masks	Mask bits for the Module-Level Flags
37-38	2	CDB Command Status	Status of current CDB command
39-40	2	Module Active Firmware Version	Module Active Firmware Version number
41	1	Fault Information	Fault cause for entering ModuleFault state
42-63	22		Reserved
64-84	21		Custom
85-117	33	Supported Applications Advertising	Applications supported by module Data Path(s)
118-125	8	Password Facilities	Password Entry and Change (mechanism only)

126-127	2	Page Mapping	Page mapping into host addressable Upper Memory
Upper Page 00h			
128	1	SFF8024IdentifierCopy	Copy of Byte 00h:0
129-144	16	VendorName	Vendor name (ASCII)
145-147	3	Vendor OUI	Vendor IEEE company ID
148-163	16	Vendor PN	Part number provided by vendor (ASCII)
164-165	2	Vendor Rev	Revision level for part number provided by vendor (ASCII)
166-181	16	Vendor SN	Vendor Serial Number (ASCII)
182-189	8	DateCode	Manufacturing Date Code (ASCII)
190-199	10	CLEICode	Common Language Equipment Identification Code (ASCII)
200-201	2	ModulePowerCharacteristics	Module power characteristics
202	1	CableAssemblyLinkLength	Cable length (for cable assembly modules only)
203	1	ConnectorType	Connector type of the media interface
204-209	6	Copper Cable Attenuation	Attenuation characteristics (passive copper cables only)
210	1	MediaLaneInformation	Supported near end media lanes (all modules)
211	1	Cable Assembly Information	Far end modules information (cable assemblies only)
212	1	MediaInterfaceTechnology	Information on media side device or cable technology
213-220	8		Reserved
221	1		Custom
222	1	PageChecksum	Page Checksum over bytes 128-221
223-255	33		Custom

Mechanical Dimension



Note:

- All dimensions are in mm.
- Unless otherwise specified, dimensional tolerance is ±0.1 mm.
- Latch color: Black.
- Cable length tolerance: ±25 mm for L < 2 m and ±50 mm for L ≥ 2 m.

Handling and Safety Precautions:

- ESD Precautions: Follow standard ESD handling procedures when handling or installing the cable assembly, particularly at the connector ends.
- Bend Radius: Do not bend the cable below the specified minimum bend radius. Avoid sharp bends or repeated bending near the connector strain-relief area.
- Cable Handling: Avoid excessive pulling, twisting, crushing, kinking, or other mechanical stress that may damage the cable or affect signal integrity.
- Installation and Removal: Use the pull tab or release mechanism when inserting or removing the cable assembly. Do not pull directly on the cable.
- Connector Protection: Keep the electrical connector contacts clean and protected from dust, moisture, and contamination when not installed.
- Cable Assembly Protection: Do not disassemble, modify, splice, or attempt to repair the cable assembly or connector housing. Replace the cable if physical damage is observed.

Ordering Information

PN	Description
O800-4Q200-AC3	800G OSFP Finned Top to 4× 200G QSFP112 Active Copper Breakout Cable,3m
O800-4Q200-AC4	800G OSFP Finned Top to 4× 200G QSFP112 Active Copper Breakout Cable,4m
O800-4Q200-AC5	800G OSFP Finned Top to 4× 200G QSFP112 Active Copper Breakout Cable,5m